ACCEL EDA merges the best features of Master Designer, TangoPRO, and significant new features. This document describes the general capabilities, new features, and enhancements in ACCEL EDA from a Master Designer perspective.

Feature	ACCEL EDA	Master Designer
Platform	Windows 3.1x, Windows 95, & Windows NT	DOS, UNIX (Sun & IBM RS6000)
Licensing	Network licenses available	UNIX only
MDI support	Multiple documents - cross probing (DDE)	Only one view at a time (DOS)
API support	DBX IN/OUT in PCB, DBX OUT in Schematic	N/A
Design Environs	All operations and utilities in one environment	Separate modules (screens) for each utility
Library	Integrated; symbols & patterns in one file	.sym & .prt in separate DOS files; requires linking
	Symbol & part browse feature	N/A
	Symbol & part creation in Sch or PCB editor	Symbol & part creation in separate editors
	Component names up to 16 characters	Component names limited to DOS 8.3 file names
ECO capability	Full ECO (forward and backward)	Reference designator, gate & pin swap only (Back)
Metafile support	Cut, copy and paste to other Windows apps	N/A
Rules-based	Sch net attributes drive the PCB & autorouter	Schematic net width rule (only) passed to PCB
Attribute definition	Fully expandable; system or user definable	Keyword specific
Attribute display	Individual attribute visibility	Layer attribute visibility
Data Manipulation	Powerful context-sensitive select tool	Multiple menu selections followed by cursor action
	Sub-select tool allows instance modification	Must push to change lib instance or query (limited)
	Add to, or remove from, block selection	Block selection final
	All data objects maskable by type & layer	Only components & wires maskable
Report generation	Formatted or comma-delimited	Formatted
Plotting	Windows drivers; plot entire file	Specific device drivers or WINplot; plot by window
Help	Windows on-line, index, hypertext, cross ref	CD ROM documentation

Feature	ACCEL Schematic	Master Schematic
Sheets	99 sheets in one design file	Individual DOS files; requires linking
Buses	Intelligent with net information	Graphical only
Hierarchy	N/A	15 hierarchical levels
Highlighting	Multiple colors; remains highlighted	Single highlights until next command invoked
Group definition	Attribute controlled	Menu function; tag components
Replace comp	All components of that type	Selected components
Scale symbols	N/A	On invocation from library
Text	Fully modifiable - TrueType font	System default; height modifiable only
Rubber-banding	Non-orthogonal	Orthogonal
Resequencing	Automatic; left to right or top to bottom	N/A

Feature	ACCEL P-CAD PCB	Master Layout
Database units	English/metric - interchangeable, auto converts	English or metric - declared prior to data input
Board size	60" x 60"	120" x 120"
Layers	99 layers; combines several MD layers in 1	100 layers; several required for 1 ACCEL EDA layer
	Global settings for solder mask & paste info	N/A
	Layer sets definable for instant hot key toggle	N/A
	Layers not containing data can be deleted	N/A
Grids	Absolute & relative; 0.0001 inch or 0.01 mm	Absolute; 0.00001 inch or 0.0001 mm
Rotation	User definable to 0.1 degree	User definable to 1.0 degree
Ratsnest display	Separate Optimize Nets command	Dynamic update to nearest pin or trace
Polygon pour	Editable polygon with modifiable properties	Fixed polygon, but can be defined with curved edges
	Automatic thermal ties & rule clearances	No automatic thermal ties & user defined clearance
	Island removal by min area, internal, subselect	Island removal by minimum area only
Padstacks	Pad styles easily defined by table entry	Customizable padstacks, but complex construction
	Pads & vias layer ordering shown in X-section	N/A
	Automatic display of thermal ties	N/A
Vias	Can be placed anywhere	Supported on vertex only
Interstitial vias	Blind & buried vias between more than 2 layers	Layer pair only; stair stepped blind & buried vias
Autoplacement	N/A	By lattice with histogram & force vectors
Autorouting	Built-in (no charge) maze router	N/A
InterRoute tool	Point-point interactive, rules driven router	N/A
Split planes	Negative polygon with signal integrity	N/A
	Automatic thermal tie or clearance of pins	N/A
Copper sharing	Drawn objects can be assigned net intelligence	N/A
Gerber data	All graphical data in a design can be automatically assigned aperture information	Aperture tables must be pre-assigned
	Gerber files can be read into the design	N/A
DXF	Z-Axis attribute support	N/A