ACCEL EDA Features

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This document lists many of the high-level features available in ACCEL EDA Version 12.00. Installation and support information can be found in the **readme.wri**.

This document is formatted so that it is suitable for both viewing on your screen and printing hardcopies. To print this document, run the File Print command while the document is loaded in Microsoft Write.

Contents

1.0 Applications

ACCEL EDA Version 12.00 consists of the following applications:

ACCEL Schematic	Schematic entry
ACCEL P-CAD PCB	PCB layout
ACCEL Tango PCB	PCB layout; up to 400 components/6 signal layers
ACCEL PRO Route	High-completion autorouter
ACCEL PRO Route 2/4	Autorouter for 2 layer or 4 layer/4000 pin designs

2.0 Features

Many of the important high-level features of ACCEL EDA are itemized below, grouped roughly by the primary impact of the compatibility. Each feature is fully described in the printed and on-line documentation provided with the product. However, ACCEL EDA includes so many capabilities for working effectively that it would be easy to overlook some of those we consider the most important.

2.1 Usability

ACCEL EDA has a “Modern” Windows look-and-feel that is consistent with other Windows applications. Its user interface includes many productivity-enhancing shortcuts and capabilities. Don't miss:

Status Line Editing. Select the current sheet/layer, grid, and line width from pick-lists. Add new grids and line widths on the fly by typing new values into the status line's edit boxes. Flip between the relative and absolute grids. Cycle-pick the current sheet/layer. Explicitly enter x- and y- coordinates for placing lines, wires, and components.

Speedy Query/Edit. Double-click (left mouse button) any item to access its context-sensitive Object Properties dialog box. This option is enabled in the Options Preferences command.

Right-mouse Access. After selecting one or more items, click the right mouse button for a context-sensitive menu of options.

Sub-selection. Press the Shift key (or Ctrl key, as set in Options Preferences for Mouse control) to select one part of an item made up of multiple items. Use this, for instance, to access a single pin, pad, or reference designator of a part or component, the signal name on a wire, or an island of a copper pour. These sub-items can be queried and edited as appropriate.

Shortcuts. Set up shortcut keyboard entries for menu commands and common actions with the Options Preferences command.

Block Selection Filters. Option Block Selection lets you choose exactly those items to be included in a block selection. Items with a button next to the check box can be specified in more detail. Click the check box until it is gray and the item's button is enabled. Choose the button to indicate the specific types of the item to be selected. Wildcards can be used in many cases.

Part and Component Browse. When placing a part or component, choose the browse button to view the item before it is placed. With the component name activated, use the up and down arrow keys to quickly view many parts or components.

Visual Pad and Via Stack-up. View the cross section of a defined pad or via style by choosing the Modify Hole Range button of the Option Pad Style command (accessed also through the Pad and Via Properties dialogs). The relative sizes of the pads and hole diameter are presented, along with the hole range and accurate layer colors.

Editing. Many individual capabilities make ACCEL EDA extremely useful for editing. Among other things, you can perform the following editing functions:

Resize items by moving one segment of a multi-segmented object or moving a "handle" (e.g., for lines, buses, wires, arcs, polygons, copper pours).

Rewire/reroute by selecting already routed wires/traces when the wire/route tool is active.

Align parts and components using the Edit Align commands.

Move objects from one layer to another with the Move to Layer command; moving traces from one signal layer to another adds or deletes vias as needed.

Move selected items by holding down the left mouse button while dragging the items to a new location ("drag-and-drop").

Copy selected items by pressing the Ctrl button while holding the mouse button down and dragging the items to the new location ("control-drag copy").

Unwind multi-line items (e.g., wires, buses, traces, polygons, copper pours, lines, splits) during placement with the backspace key.

Move or rotate selected items using a Selection Point as a reference.

Place a component, identified by its reference designator, to the current cursor location.

2.2 Configurability

Configure ACCEL EDA to your own specifications with the following features:

Configuration Options. Three commands are dedicated to presenting a range of setup, display, and user-preference options. They include options for workspace configuration, auto save, user-specified file viewer, ECO control, default units, pan and zoom control, connector styles, user-defined hot keys, mouse operation, shortcut keys, color control, and much more.

Net Classes. Net classes may be named, saved, modified, and included in the netlist.

Hierarchical Design Rules. DRC checks clearances using hierarchical inheritance rules for class-to-class, net, net class, and design level precedence. Net classes and clearance values are passed to the SPECCTRA router.

True Type Fonts. True Type fonts are available for all text on Schematic sheets.

Symbol Representations. Symbols may be displayed using their IEEE & DeMorgan alternatives.

Layer Sets. Sets of layers can be defined to assist set-up for display, printing, Gerber, NC Drill, DXF Out, and active layers.

Pad/Layer Ordering. Layer order is supported and presented visually. DRC, NC drill, and Gerber functions appropriately use the layer order and the hole range.

Network licensing. Network licenses are available for ACCEL Schematic, ACCEL P-CAD PCB, and ACCEL PRO Route on the Windows 3.1 operating system.

2.3 Power

ACCEL EDA offers many features to facilitate the design of high-end PCBs. Here are a few:

Copper Pour. Copper pours include island detection and removal based on island size, by sub-selecting islands, or if an island is an interior island. Connectivity is correct, traces added to a pour are automatically plowed, and the backoff may be set to be smooth or coarse. The hierarchical clearance rules can be used to backoff different amounts from different signals.

Split Plane Support. Power and ground planes can be split and assigned to multiple nets. Splits are defined by polygonal areas and may be given unique colors. Pins are automatically tied and DRC supports the connections. The splits are drawn, printed, and photoplotted in the negative.

Interactive Routing. An interactive, shape-based, assisted routing tool is included in ACCEL P-CAD PCB. "InterRoute" avoids obstacles, provides copper hugging, and honors all routing, net, and class clearances. Guide the route path or allow the tool to choose the path. Vias are autoplaced with a layer change. Redundant tracks are removed (“backtracking”).

QuickRoute. Built-in maze autorouter.

Blind & Buried Vias. Blind and buried vias can be defined with different pad shapes and sizes per layer, with user-defined hole diameter and hole range. DRC, NC drill, and Gerber functions appropriately use the defined stack up.

Orthogonal Modes. Switch between orthogonal, 45 degree, and curved (PCB) wires or traces on the fly by pressing the O key when placing wires or traces. (Pressing the F key during placement flips the item.)

Abutment Routing. Quickly create multiple wire connections between two symbols by overlapping the symbol pins and then moving one symbol away from the other.

Pin and Gate Swapping. Optimize connection lengths by swapping pins and or gates using the Optimize Nets command in the PCB applications.

2.4 Correctness by Design

ACCEL EDA follows a "correct by design" philosophy to help eliminate errors. This leaves more time to focus on completing the design itself. The following are a few of the features that help maintain design correctness:

Resolution. ACCEL EDA has a sub-micron database. Items can be rotated to one tenth of one degree. Values are accurately converted between English and metric units with no round-off error.

Rules Checking. ACCEL EDA offers comprehensive electrical and design rules checking including clearance checks against the full set of hierarchical rules, copper pour violations, hole range and drill errors, padstack inconsistencies, plane layer connectivity, electrical shorts and isolated copper on signal and plane layers, and many more. Error indicators contain detailed information about their corresponding violations.

Plane Connections. Thermal connections are automatically made to tie signals to planes.

Apertures and Drill Assignments. Aperture and drill assignments are made automatically or can be overridden.

Packaging. ACCEL EDA packages parts into components. Reference designators are automatically assigned and are maintained to be unique. Shortcuts are available to override the part and RefDes assignments and force a part into a new package.

WYSIWYG Output. What-You-See-Is-What-You-Get". Items are displayed accurately to match their Gerber, drill, and report output.

Wire Splitting. A new signal is created and automatically named when an in-line symbol is placed in the middle of an existing wire, thus splitting the wire.

On-line DRC. Design rule checking can be enabled to run while the design is being constructed.

2.5 Integration

ACCEL EDA's schematic, PCB and autorouting applications are tightly integrated in many ways. Don't miss the following:

Attributes. ACCEL EDA supports the creation, editing, and display of component, net, and design level attributes for engineering specs. Attributes may be system or user-defined, and can be transferred from schematic to PCB so the data is consistent and entered only once. Many attributes are recognized by the autorouters.

Integrated Libraries. ACCEL EDA supports integrated libraries, containing components having electrical data, a symbolic representation, and a physical footprint. This arrangement simplifies and maintains consistency between the schematic and PCB for netlist loading, ECO processing, pin and gate swapping, and cross-probing.

Library Management. Simultaneously view all component data in multiple windows when creating or modifying components. Includes graphic views of the pattern and symbol, a spreadsheet view of pin information, and a dialog box of component data. Pins, pads, and spreadsheet rows are highlighted to match selections within any of the browse windows. Much of the data is automatically filled. Error checking can be done before saving the component.

Pattern and Symbol Creation. Symbol and pattern graphics are built within the schematic and PCB applications respectively. Create a component on the fly at the same time (it will have only electrical information and the symbol or pattern; the graphics for the other application can be added in the Library Manager). Symbols and patterns can be created once and re-used to define additional components.

Library Report. Query and report on components from one or more libraries having selected attributes, patterns, types, or symbols. Wildcards can be used to specify desired components. Sort output and generate a formatted report or a list using the comma-separated file format.

ECOs. Engineering change orders can be captured and applied backward and forward between schematic and PCB applications to keep them in synch. Changes include those to reference designators, nets, net nodes, parts, components and attributes.

Cross-probing. Cross-application highlighting locates corresponding nets and components in the schematic and PCB designs. Multiple parts are highlighted if they correspond to a single component.

Router Integration. ACCEL EDA offers seemless integration between the PCB layout and optional PRO Route applications. A "DO Wizard" is provided to simplify the interface with the Cooper and Chyan SPECCTRA autorouters.

2.6 Manufacturability

The following are a few of the many capabilities ACCEL EDA has available to assist in generating accurate and usable output:

Dimensioning. Basic dimensioning capabilities include baseline, point-to-point, center, leader, radial, diameter, and angular dimensions.

Mitering. Curved and 45 degree miters are offered for traces in PCB.

Gerber Viewer. Read a Gerber output file into the active PCB design. With the corresponding layers active switch between layers to view changes and deletions made since the Gerber file was created.

NC Drill. Integrated setup, tool assignment, and format for NC Drill support.

Points. ACCEL EDA supports glue dots and pick-and-place points for report generation and manufacturing output.

Assembly and Paste Layer Artwork. The setup for generating this artwork is user-defined and can be saved for re-use.

Report Generation. ACCEL EDA provides a comprehensive list of output reports.

Setup. Save and restore your output setup configuration.

DXF. Input and output Design Interchange Format (DXF) is supported for interfacing popular mechanical CAD programs. Includes z-axis component support for output.

2.7 Inter-operability

ACCEL EDA supports many methods of interfacing to external programs. Using the following capabilities, the opportunities are virtually endless:

Cut/Copy. Graphics are cut to the clipboard in bitmap form (Windows metafile format) for pasting in other Windows programs such as Word, AutoCAD, FrameMaker, etc. This facilitates design documentation.

Printing. ACCEL EDA uses Windows-supported printers.

Multiple Document Interface (MDI). MDI is available to view multiple designs or multiple views of any design at one time.

ASCII Files. ASCII versions of ACCEL EDA schematic and PCB design files, as well as library files, can be input and output. Master Designer Version 6.0 - 8.5 PDIF files are accepted and V8.5 PDIF files are exported including netlist attributes. Many PDIF interface programs are available from ACCEL resellers and third party developers.

Application Programming Interface (API). ACCEL's API, "DBX", includes functions to extract schematic and PCB design data, and write PCB data, while the design is open. The functions may be called from Visual Basic, C, or C++ Windows programs. Many valuable sample programs are provided in the UTILS subdirectory.

Third Party Interfaces. Tightly coupled interfaces are available to Cooper and Chyan's SPECCTRA autorouters, Viewlogic's WorkView Office schematic, and Advanced CAM Technologies' CAM350 family of CAM tools. Many other interfaces are available through ACCEL's local resellers and other third party developers.