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Recommendation O.151

ERROR PERFORMANCE MEASURING EQUIPMENT FOR DIGITAL SYSTEMS AT THE PRIMARY BIT RATE AND ABOVE

(Geneva, 1976; amended Geneva, 1980, Malaga-Torremolinos, 1984 and Melbourne, 1988)

The requirements for the characteristics of bit-error performance measuring equipment which are described below must be adhered to in order to ensure compatibility between equipments standardized by the CCITT, and produced by different manufacturers.

1 General

The equipment is designed to measure the bit-error performance of digital transmission systems by the direct comparison of a pseudorandom test pattern with an identical locally generated test pattern. In addition the capability to measure errored time intervals is provided.

2 Test patterns

2.1 *Pseudorandom pattern for systems using a 2 pattern length*

This pattern is to be produced by means of a shift register incorporating appropriate feedback (see Figure 1/O.151 and Table 1/O.151):
Number of shift register stages 15
Pattern length 2^{15} — 1 = 32 | 67 bits

Feedback taken from the 14th and 15th stage via an exclusive-OR-gate to the first stage Longest sequence of zeros 15 (inverted signal)

2.2 *Pseudorandom pattern for systems using 2 pattern length*

This pattern is to be produced by means of a shift register incorporating appropriate feedback (see Figure 2/O.151):
Number of shift register stages 23
Pattern length 2^{23} — 1 = 8 | 88 | 07 bits

This Recommendation is the joint responsibility of Study Groups IV, XVII and XVIII.

Feedback taken from the 18th and 23rd stages via an exclusive-OR-gate to the first stage Longest sequence of zeros 23 (inverted signal)

Table 1/O.151 [T1.151], p.

Figure 1/O.151, p.

Figure 2/O.151 p.

2.3 *Pseudorandom pattern for systems using 2 pattern length*

This pattern may be generated by a twenty stage shift register with feedback taken from the seventeenth and twentieth stages. The output signal is taken from the twentieth stage, and an output bit is forced to be a ‘‘one’’ whenever the next 14 bits are all ‘‘zero’’.

The quasi-random sequence satisfies the following:

$$Q_{n\d+1}(k+1) = Q_n(k),$$
$$n = 1, 2, \ldots, 19,$$

$$Q_1(k+1) = Q_{1\d7}(k) \oplus Q_{2\d0}(k), \text{ and}$$

$$RD(k) = Q_{2\d0}(k) + Q_6(k) + \ldots + Q_{1\d9}(k)$$

where

$Q_n(k)$ = Present state for n th stage

$Q_n(k+1)$ = Next state for n th stage

$RD(k)$ = Present value of output

+ = a logic OR operation

$\oplus$ = a logic EXCLUSIVE OR operation

( ) = a logic NEGATION operation.

2.4 *Fixed patterns (optional)*

Fixed patterns of all ones and alternating ones and zeros may be provided.

3 Bit rate

The bit rates in accordance with CCITT Recommendations are indicated in Table 2/O.151.

H.T. [T2.151]

TABLE 2/O.151

Bit rates, pertinent Recommendations and pseudo random test patterns

Bit rates (kbit/s) Recommendations corresponding to multiplex system } Recommendations corresponding to digital line section/line system }	{ { Bit rate tolerance	Test pattern		
1 | 54 G.911 [8], G.951 [9], G.955 [10] } ± 50 | (mu | 0^{D}lF261^{6} } 2^{15}—1, 2^{20}—1 }	G.733 [1] { {	{		
2 | 48 G.921 [11], G.952 [12], G.956 [13] } ± 50 | (mu | 0^{D}lF261^{6} }	G.732 [2] { 2^{15}—1	{		
6 | 12 G.912 [14], G.951 [9], G.955 [10] } ± 30 | (mu | 0^{D}lF261^{6} } 2^{15}—1, 2^{20}—1 }	G.743 [3] { {	{		
8 | 48 G.921 [11], G.952 [12], G.956 [13] } ± 30 | (mu | 0^{D}lF261^{6} }	G.742 [4], G.745 [5] { 2^{15}—1	{		
32 | 64 G.913 [15], G.953 [16], G.955 [10] } ± 10 | (mu | 0^{D}lF261^{6} } 2^{15}—1, 2^{20}—1 }	G.752 [6] { {	{		
34 | 68 G.921 [11], G.954 [17], G.956 [13] } ± 20 | (mu | 0^{D}lF261^{6} }	G.751 [7] { 2^{23}—1	{		
44 | 36 G.914 [18], G.953 [16], G.955 [10] } ± 20 | (mu | 0^{D}lF261^{6} } 2^{15}—1, 2^{20}—1 }	G.752 [6] { {	{		
139 | 64 G.921 [11], G.954 [17], G.956 [13] } ± 15 | (mu | 0^{D}lF261^{6} }	G.751 [7] { 2^{23}—1	{		

Table 2/O.151 [T2.151], p.

Note — Normally only the appropriate combination of bit rates — either 2048 kbit/s, 8448 kbit/s, etc. or 1544 kbit/s, 6312 kbit/s, etc. — will be provided in a given instrumentation.

4 Interfaces

The interface characteristics (impedances, levels, codes, etc.) should be in accordance with Recommendation G.703 [19].

In addition to providing for terminated measurements the instrumentation shall also be capable of monitoring at protected test points on digital equipment. Therefore, a high impedance and/or additional gain should be provided to compensate for the loss at monitoring points already provided on some equipments.

5 Error-ratio measuring range

The receiving equipment of the instrumentation should be capable of measuring bit-error ratios in the range 10^{D}lF261^{3} to 10^{D}lF261^{8}. In addition, it should be possible to measure bit-error ratios of 10^{D}lF261^{9} and 10^{D}lF261^{10}; this can be achieved by providing the capability to count cumulative errors.

6 Mode of operation

The mode of operation should be such that the signal to be tested is first converted into a unipolar (binary) signal in the error measuring instrument and subsequently the bit comparison is made also with a reference signal in binary form.

Facilities may *optionally* | e provided to allow the direct comparison at line code (e.g. AMI or HDB-3) with correspondingly coded reference signals. In the case of such measurements polarity distinction is possible, so that errors caused by the injection or omission of positive or negative pulses can be determined separately.

7 Measurement of errored time intervals

The instrument shall be capable of detecting errored seconds and other errored or error-free time intervals as defined in § 1.4 of Recommendation G.821 [20] and of deriving error performance reduced to 64 kbit/s in accordance with Annex D to Recommendation G.821 [20] observation period from 1 minute to 24 hours, or continuous, shall be counted and displayed.

For this measurement the error detection circuits of the instrument shall be controlled by an internal timer which sets intervals of equal length and which operates independently of the occurrence of errors.

8 Operating environment

The electrical performance requirements shall be met when operating at the climatic conditions as specified in Recommendation O.3, § 2.1.

References

[1] CCITT Recommendation *Characteristics of primary PCM multiplex equipment operating at 1544 kbit/s* , Vol. III, Rec. G.733.

[2] CCITT Recommendation *Characteristics of primary PCM multiplex equipment operating at 2048 kbit/s* , Vol. III, Rec. G.732.

[3] CCITT Recommendation *Second-order digital multiplex equipment operating at 6312 kbit/s and using positive justification* , Vol. III, Rec. G.743.

[4] CCITT Recommendation *Second-order digital multiplex equipment operating at 8448 kbit/s and using positive justification* , Vol. III, Rec. G.742.

[5] CCITT Recommendation *Second-order digital multiplex equipment operating at 8448 kbit/s and using positive/zero/negative justification* , Vol. III, Rec. G.745.

[6] CCITT Recommendation *Characteristics of digital multiplex equipments based on a second-order bit rate of 6312 kbit/s and using positive justification* , Vol. III, Rec. G.752.

[7] CCITT Recommendation *Digital multiplex equipments operating at the third-order bit rate of 34 | 68 kbit/s and the fourth-order bit rate of 139 | 64 kbit/s and using positive justification* , Vol. III, Rec. G.751.

[8] CCITT Recommendation *Digital line sections at 1544 kbit/s* , Vol. III, Rec. G.911.

[9] CCITT Recommendation *Digital line systems based on the 1544 kbit/s hierarchy on symmetric pair cables*, Vol. III, Rec. G.951.

[10] CCITT Recommendation *Digital line systems based on the 1544 kbit/s hierarchy on optical fibre cables* , Vol. III, Rec. G.955.

[11] CCITT Recommendation *Digital sections based on the 2048 kbit/s hierarchy* , Vol. III, Rec. G.921.

[12] CCITT Recommendation *Digital line systems based on the 2048 kbit/s hierarchy on symmetric pair cables* , Vol. III, Rec. G.952.

[13] CCITT Recommendation *Digital line systems based on the 2048 kbit/s hierarchy on optical fibre cables* , Vol. III, Rec. G.956.

[14] CCITT Recommendation *Digital line sections at 6312 kbit/s* , Vol. III, Rec. G.912.

Error performance evaluation at bit rates other than 64 kbit/s is under study.

[15] CCITT Recommendation *Digital line sections at 32 | 64 kbit/s* , Vol. III, Rec. G.913.

[16] CCITT Recommendation *Digital line systems based on the 1544 kbit/s hierarchy on coaxial pair cables* , Vol. III, Rec. G.953.

[17] CCITT Recommendation *Digital line systems based on the 2048 kbit/s hierarchy on coaxial pair cables* , Vol. III, Rec. G.954.

[18] CCITT Recommendation *Digital line sections at 44 | 36 kbit/s* , Vol. III, Rec. G.914.

[19] CCITT Recommendation *Physical/electrical characteristics of hierarchical digital interfaces* , Vol. III, Rec. G.703.

[20] CCITT Recommendation *Error performance on an international digital connection forming part of an integrated services digital network* , Vol. III, Rec. G.821.

ERROR PERFORMANCE MEASURING EQUIPMENT FOR 64 kbit/s PATHS

(Malaga-Torremolinos, 1984; amended, Melbourne, 1988)

The requirements for the characteristics of a bit-error performance measuring equipment which are described below must be adhered to in order to ensure compatibility between equipments standardized by the CCITT, and produced by different manufacturers.

1 General

The set is designed to measure the bit-error performance of digital paths (operating at 64 kbit/s) by the direct comparison of a pseudorandom test pattern with an identical locally generated test pattern.

2 Test patterns

2.1 *Pseudorandom pattern*

This pattern is to be produced by means of a shift register incorporating appropriate feedback (see Figure 1/O.152):
Number of shift register stages 11
Pattern length $2^{11} - 1 = 2047$ bits

Feedback taken from the outputs of the 9th and 11th stage via an exclusive-OR-gate to the first stage Longest sequence of zeros 10 (non-inverted signal)

Note 1 — In the case of international testing where the measurement includes systems based on 1544 kbit/s it is necessary to modify the test sequence in such a way that more than seven consecutive ‘‘0’’-bits are avoided. This is achieved by forcing the output signal to ‘‘1’’ whenever the next 7 bits of the sequence are all zeros.

Note 2 — It is recommended to use the test pattern of 2047 bit length also at other bit rates in the range 48 kbit/s to 168 kbit/s.

Figure 1/O.152, p.

2.2 *Fixed patterns* | optional)

Fixed patterns of all ones (. | | | 111 | | |) and alternating ones and zeros (. | | | 010 | | |) may be provided.

3 Bit rate

Bit rate in accordance with CCITT Recommendations G.703, § 1 [1] and V.36 [2] of 64 kbit/s:

a) bit rate tolerance (Recommendation G.703 [1]): ± | 00 | (mu | 0^{D}lF261^{6},

b) bit rate tolerance (Recommendation V.36 [2]), optional: ± | 0×10^{D}lF261^{6}.

4 Interfaces

The interface characteristics (impedances, levels, codes, etc.) should be in accordance with Recommendations G.703 [1], I.430 [7] (optional) and V.11 [3] (optional).

In addition to providing for terminated measurements the measuring set shall also be capable of monitoring at protected test points on digital equipment. Therefore, a high impedance and/or additional gain must be provided to compensate for the loss at monitoring points already provided on some equipments.

4.1 *Interfaces corresponding to Recommendation G.703* [1]

Three interfaces shall be provided:

a) a codirectional interface in accordance with Recommendation G.703, § 1.2.1 [1],

b) a centralized clock interface in accordance with Recommendation G.703, § 1.2.2 [1],

c) a contradirectional interface in accordance with Recommendation G.703, § 1.2.3 [1].

4.2 *Method of clock synchronization*

The following modes of synchronization shall be selectable:

a) Lock the digital generator clock rate to that at the input of the receive side of the measuring set (for the codirectional interface).

b) Allow the generator clock to free run within the overall allowed frequency tolerances.

c) Lock the digital generator clock rate to an external clock signal. (Configuration of input for external clock in accordance with Recommendation G.703 [1].)

4.3 *Interface corresponding to Recommendation I.430 [7]*

For further study. This study should include means for obtaining access to the individual 64 kbit/s channels at the S and T interface points.

4.4 *Interface corresponding to Recommendation V.11 [3]*

As an option an interface in accordance with Recommendation V.11 [3] shall be provided.

5 Bit-error-ratio measuring range

The receiving equipment of the set should be capable of measuring bit-error ratios in the range 10^{D}lF261^{2} to 10^{D}lF261^{7}. The measurement time should be sufficiently long to achieve accurate measurements. In addition, it should be possible to measure bit-error ratios smaller than 10^{D}lF261^{7}; this can be achieved by providing the capability to count cumulative errors.

6 Block-error ratio measurements

Optionally, the instrument should be capable to perform block-error measurements in addition to the bit-error measurements. If provided it should be possible to measure block-error ratios in the range 10^{D}lF261^{0} to 10^{D}lF261^{5} when using the pseudorandom test pattern with a block length of 2047 bits.

7 Mode of operation

The mode of operation should be such that the signal to be tested is first converted into a unipolar (binary) signal in the error measuring instrument and subsequently the bit comparison is made also with a reference signal in binary form.

8 Error evaluation

8.1 *Measurement of errored time intervals*

The instrument shall be capable of detecting errored seconds and other errored or error-free time intervals as defined by Recommendation G.821 [4]. The number of errored or error-free time intervals in a selectable observation period from 1 minute to 24 hours, or continuous, shall be counted and displayed.

For this measurement the error detection circuits of the instrument shall be controlled by an internal timer which sets intervals of equal length and which operates independently of the occurrence of errors.

8.2 *Measurement of short-term mean error ratio*

8.2.1 It shall be possible to record the time intervals as defined in Recommendation G.821 [4], during which the bit-error ratio is less than 1 | (mu | 0^{D}lF261^{6}.

8.2.2 It shall be possible to record the one-second intervals during which the bit-error ratio is less than 1 | (mu | 0^{D}lF261^{3}.

9 Recording of measurement results

As an option an interface shall be provided which allows connecting external equipment for further processing the measuring results.

The interface shall comply with Recommendation V.24 [5] or the interface bus according to IEC Publication 625 [6].

10 Operating environment

The electrical performance requirements shall be met when operating at the climatic conditions as specified in Recommendation O.3, § 2.1.

References

[1] CCITT Recommendation *Physical/electrical characteristics of hierarchical digital interfaces* , Vol. III, Rec. G.703.

[2] CCITT Recommendation *Modems for synchronous data transmission using 60-108 kHz group band circuits* , Vol. VIII, Rec. V.36.

[3] CCITT Recommendation *Electrical characteristics for balanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications* , Vol. VIII, Rec. V.11.

[4] CCITT Recommendation *Error performance on an international digital connection forming part of an integrated services digital network* , Vol. III, Rec. G.821.

[5] CCITT Recommendation *List of definitions for interchange circuits between data terminal equipment and data circuit-terminating equipment* , Vol. VIII, Rec. V.24.

[6] IEC Publication 625 *An Interface system for programmable measuring instruments (byte serial, bit parallel)* .

[7] CCITT Recommendation *Basic user-network interface-Layer/Specification* , Vol. III, Recommendation I.430.

Recommendation O.153

BASIC PARAMETERS FOR THE MEASUREMENT OF ERROR PERFORMANCE AT BIT RATES BELOW THE PRIMARY RATE

(Melbourne, 1988)

The requirements for the characteristics of error measuring instrumentation which are described below must be adhered to in order to ensure compatibility between equipments standardized by the CCITT and produced by different manufacturers.

While requirements are given for the instrumentation, the realization of the equipment configuration is not covered and should be given careful consideration by the designer and user. In particular, it is not required that all features listed below shall be provided in one instrument. Administrations may select those functions which correspond best to their applications.

When selecting functions, Administrations may also consider other Recommendations dealing with error measuring equipment, e.g. Recommendations O.151 and O.152.

1 General

The instrumentation is designed to measure the error performance on data circuits operating at bit rates between 0.050 and 168 kbit/s. The measurement is based on the direct comparison of specified test patterns which are transmitted through the circuit under test with identical patterns generated at the receive side. Synchronous and asynchronous operation shall be possible.

2 Test patterns

The following test patterns are standardized (see Note):

Note — The use of certain test patterns may be restricted to synchronous or asynchronous operation only. It shall be possible to transmit the patterns for an unlimited time.

2.1 *511-bit pseudorandom test pattern*

This pattern is primarily intended for error measurements at bit rates up to 14 | 00 bit/s (see § 3.1 below).

The pattern may be generated in a nine-stage shift-register whose 5th and 9th stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage. The pattern begins with the first ONE of 9 consecutive ONES.

Number of shift-register stages 9

Length of the pseudorandom sequence $2^9 - 1 = 511$ bits

Longest sequence of zeros 8 (non-inverted signal)

2.2 *2047-bit pseudorandom test pattern*

If provided, this pattern is primarily intended for error measurements at bit rates of 64 kbit/s (see § 3.3 below).

The pattern may be generated in an eleven-stage shift-register whose 9th and 11th stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage. (See also Rec. O.152)

Number of shift-register stages 11

Length of the pseudorandom sequence $2^{11} - 1 = 2047$ bits

Longest sequence of zeros 10 (non-inverted signal)

2.3 *1048.575 kbits pseudorandom test pattern*

This pattern is primarily intended for error measurements at bit rates up to 72 kbit/s (see § 3.2 below).

The pattern may be generated in a twenty-stage shift-register whose 3rd and 20th stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage.

Number of shift-register stages 20

Length of the pseudorandom sequence $2^{20} - 1 = 1048.575$ kbits

Longest sequence of zeros 19 (non-inverted signal)

Note — This test pattern is not identical with the pattern of the same length specified in Recommendation O.151.

2.4 *Fixed test patterns* | for continuity tests)

— Permanent space

— Permanent mark

— Alternating space/mark with a ratio of: 1 | | , 1 | | , 1 | | , 3 | | , 7 | |

— ‘‘Quick brown fox’’ — text (QBF) [1] (asynchronous mode only).

2.5 *Programmable test patterns*

A freely programmable pattern with a length of at least 1024 bits is recommended.

3 Bit rates

The instrumentation shall provide for measurements at bit rate ranges as specified in the categories below.

3.1 *Data transmission via telephone-type circuits using modems*

— Bit rate range 50 bit/s to 19 | 00 bit/s.

(See Recommendations V.5 [2] and V.6 [3] for details).

Note — Modems operating at bit rates above 14 | 00 bit/s are not covered by CCITT Recommendations.

3.2 *Data transmission via group-band circuits using wideband modems*

— Bit rate range 48 kbit/s to 168 kbit/s.

(See Recommendations V.36 [4] and V.37 [5] for details).

3.3 *Data transmisison at and above 64 kbit/s*

With regard to error performance measurements at 64 kbit/s, relevant information can be found in Recommendation O.152.

Information on measurements at primary bit rates is contained in Recommendation O.151.

3.4 *Deviation from nominal bit rate*

For bit rates up to 9600 bit/s the maximum deviation from the nominal bit rate shall be 0.01% if timing is not derived from the object under test.

For the higher bit rates the maximum deviation shall be 0.002% if timing is not derived from the object under test.

3.5 *Clock sources*

Clock signals are provided through the interface, via an external synchronisation input or from an internal clock generator.

4 Interfaces

Depending on the application and the bit rate, one or several of the following interfaces shall be provided:

— Interface according to Recommendation V.10 (X.26) [6]

— Interface according to Recommendation V.11 (X.27) [7]

— Interface according to Recommendations V.24/V.28 [8] [9]

— Interface according to Recommendation V.35 [10]

— Interface according to Recommendation V.36 [4]

— Interface according to Recommendations X.21/X.24 [11] [12].

5 Modes of operation

The instrumentation must fully simulate the characteristics of a DTE and/or a DCE in half duplex and/or full duplex mode. This includes the relevant software or hardware handshaking procedures. In synchronous half duplex mode, the test pattern shall be preceded by two or more leading pads (i.e. characters with alternating mark and space bits) to enable clock recovery. These pads shall be followed by two or more block-synchronization characters.

If the mode of operation requires, it shall be possible to select the parity check conditions even, odd, mark and space.

Note — The insertion of parity check bits is normally not possible when using pseudorandom test patterns.

6 Bit of synchronization

Two modes of synchronization shall be possible:

— Synchronization by means of a timing signal derived from the object under test (e.g. from a modem operating in the synchronous mode).

— Synchronization from the transitions of the received test signal (e.g. when a modem is operating in the nonsynchronous mode).

7 Codes

For encoding the QBF-text or a freely programmable pattern, the following data signal code shall be provided:

— CCITT Alphabet No. 5 with 7 bits/character [13]

For asynchronous operation 1 or 2 stop bits shall be selectable.

8 Error measurements and error evaluation

8.1 *Bit error measurements*

The range for error ratio measurements shall be 10^{-2} to 10^{-7}. The measurement time shall be sufficiently long to achieve accurate results.

Error ratios smaller than 10^{-7} can be observed by providing the capability to count cumulative errors.

8.2 *Block error measurements*

It shall be possible to perform block error measurements. The block length shall be selectable to 1000 or 10 | 00 bits or shall be equal to the length of the pseudorandom sequence used for the error test. In addition, a block length of 32 | 68 bits shall be provided for measurements at bit rates above 14.4 kbit/s.

The range for block error ratio measurements shall be 10^{-0} to 10^{-5} with measurement times being sufficiently long to achieve accurate results.

8.3 *Simultaneous measurements*

It shall be possible to perform bit error ratio and block error ratio measurements simultaneously.

8.4 *Error performance evaluation*

The instrumentation shall be capable of detecting errored seconds. The number of errored and error-free time intervals in a selectable time period from 1 minute to 24 hours, or continuous, shall be counted and displayed.

For this measurement the error detection circuits of the instrumentation shall be controlled by an internal timer which sets intervals of equal length and which operates independently of the occurrence of errors.

The measurement of other error performance parameters and the application of Recommendation G.821 [14] are under study.

9 Measurement of distortion

If the instrumentation provides for distortion measurements, the following specifications are applicable:

9.1 *Measurement of individual distortion*

The degrees of early and late individual distortion shall be measured when the instrumentation is operating in the mode in which synchronization is derived from transitions in the received test signal.

When using pseudorandom test signals, the measuring error shall be less than ± | %.

9.2 *Measurement of bias distortion*

The instrumentation shall measure bias distortion on reversals (alternating space/mark with a ration of 1 | |).

In this mode, the measuring error shall be less than ± | %.

10 Remote control, recording of measurement results

As an option, an interface shall be provided which allows remote control of the instrumentation and further processing of the measuring results.

If provided, the interface shall comply with the interface bus according to IEC Publication 625 [15] or with Recommendation V.24 [8].

11 Operating environment

The electrical performance requirements shall be met when operating at climatic conditions as specified in Rec. O.3, § 2.1.

References

[1] CCITT Recommendation *Standardization of international texts for the measurement of the margin of start-stop equipment* , Vol. VII, Rec. R.52.

[2] CCITT Recommendation *Standardization of data signalling rates for synchronous data transmission in the general switched telephone network* , Vol. VIII, Rec. V.5.

[3] CCITT Recommendation *Standardization of data signalling rates for synchronous data transmission on leased telephone-type circuits* , Vol. VIII, Rec. V.6.

[4] CCITT Recommendation *Modems for synchronous data transmission using 60-108 kHz group band circuits* , Vol. VIII, Rec. V.36.

[5] CCITT Recommendation *Synchronous data transmission at a data signalling rate higher than 72 kbit/s using 60-108 kHz group band circuits* , Vol. VIII, Rec. V.37.

[6] CCITT Recommendation *Electrical characteristics for unbalanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications* , Vol. VIII, Rec. V.10.

[7] CCITT Recommendation *Electrical characteristics for balanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications* , Vol. VIII, Rec. V.11.

[8] CCITT Recommendation *List of definitions for interchange circuits between data terminal equipment and data circuit-terminating equipment* , Vol. VIII, Rec. V.24.

[9] CCITT Recommendation *Electrical characteristics for unbalanced double-current interchange circuits* , Vol. VIII, Rec. V.28.

[10] CCITT Recommendation *Data transmission at 48 kbit/s using 60-108 kHz group band circuits* , Vol. VIII, Rec. V.35.

[11] CCITT Recommendation *Interface between data terminal equipment (DTE) and data circuit-terminating equipment (DCE) for synchronous operation on public data networks* , Vol. VIII, Rec. X.21.

[12] CCITT Recommendation *List of definitions for interchange circuits between data terminal equipment (DTE) and data circuit-terminating equipment (DCE) on public data networks* , Vol. VIII, Rec. X.24.

[13] CCITT Recommendation *International Alphabet No. 5* , Vol. VII, Rec. T.50.

[14] CCITT Recommendation *Error performance of an international digital connection forming part of an integrated digital network* , Vol. III, Rec. G.821.

[15] IEC Publication 624 *An interface system for programmable measuring instruments (byte serial, bit parallel)* .

Recommendation O.161

IN-SERVICE CODE VIOLATION MONITORS FOR DIGITAL SYSTEMS

(Geneva, 1980; amended Malaga-Torremolinos, 1984)

1 General

This specification describes an in-service code violation monitor for the first and second level in the digital transmission hierarchy.

The pseudoternary codes to be monitored are alternate mark inversion (AMI), high density bipolar with a maximum of 3 consecutive zeros (HDB3), B6ZS and B8ZS.

2 Definition of code violation

2.1 *AMI*

Two consecutive marks of the same polarity. This may not be the absolute number of errors.

2.2 *HDB3*

Two consecutive bipolar violations of the same polarity. This may not be the absolute number of errors.

According to the definitions of code violations in this Recommendation it should be taken into account that the code violation monitor will not detect zero sequences which violate the relevant coding rules.

2.3 *B6ZS*

Two consecutive marks of the same polarity excluding violations caused by the zero substitution code. This may not be the absolute number of errors.

2.4 *B8ZS*

Two consecutive marks of the same polarity excluding violations caused by the zero substitution code number or errors.

3 Input signal

3.1 *Interface*

The code violation monitor shall be capable of operating at the following bit rates and corresponding interface characteristics as described in the appropriate paragraphs of Recommendation G.703 [1]:

a) 1544 kbit/s;

b) 6312 kbit/s;

c) 2048 kbit/s;

d) 8448 kbit/s.

3.2 *Instrument operation*

3.2.1 The instrument may be equipped to monitor only one or two of the listed codes and operate at the appropriate bit rates for those codes.

3.3 *Input sensitivity*

3.3.1 The instrument is required to operate satisfactorily under the following input conditions.

3.3.1.1 Input impedances and levels in accordance with Recommendation G.703 [1].

3.3.1.2 The instrument shall also be capable of monitoring at protected test points on digital equipment. Therefore, a high impedance input and/or additional gain of 30 dB (40 dB — see Note) shall be provided to compensate for the loss at the monitoring points already provided on some equipment.

Note — As an option for instruments operating at an interface of 1544 kbit/s corresponding to the Recommendation cited in [1], the additional gain, where provided, shall be 40 dB.

3.3.1.3 Additionally, the instrument is required to operate satisfactorily, in both the terminated and monitor mode, when connected to an interface output in accordance with Recommendation G.703 [1] via a length of cable which can have an insertion loss of 0 dB to 6 dB at the half bit rate of the signal. The insertion loss of the cable at other frequencies will be proportional to $\sqrt{fIf\ |}$.

3.4 *Input impedance*

3.4.1 The instrument shall have a return loss better than 20 dB under the conditions listed in Table 1/O.161.

H.T. [T1.161]

TABLE 1/O.161

{ Instrument operating at (kbit/s) }	Test conditions	
1544	100 ohms, nonreactive	20 kHz to 1.6 MHz
2048	75/120/130 ohms, nonreactive	40 kHz to 2.5 MHz
6312	75/110 ohms, nonreactive	100 kHz to 6.5 MHz
8448	75 ohms, nonreactive	100 kHz to 10.0 MHz

Table 1/O.161 [T1.161], p.

3.5 *Signal input gating*

3.5.1 The instrument shall incorporate a sampling circuit, operated from the incoming digital signal, such that the instrument senses only the voltages which are present during a short gating period at the midpoint of each digit time slot.

3.6 *Input jitter tolerance*

3.6.1 The instrument shall be able to tolerate the lower limit of maximum tolerable input jitter specified in the appropriate paragraph of Recommendation G.703 [1].

4 Display

4.1 The instrument shall incorporate an indicator to show the presence of a digital signal of correct amplitude and bit rate.

4.2 The code violation rate shall be indicated in the range 1 in 10^3 to at least 1 in 10^6. Indication of code violations, occurring in the input signal and detected as defined in § 2 above, shall be determined by counting the number of code violations that occur during the period of at least 10^6 digit time slots.

4.3 It shall be possible to indicate the sum of the code violations. This facility will not be required at the same time as the code violation rate is being counted and displayed.

4.4 The count capacity shall be 99 999 and a separate indicator shall be given if the count exceeds this figure.

4.5 The counting sequence shall be started by operating a ‘‘start’’ control and shall be stopped by a ‘‘stop’’ control.

4.6 The counter, and its display, shall be capable of being reset.

5 Instrument check

5.1 A check facility shall be provided. This facility is to enable a check to be made of the display, counter and recorder output and optionally of the instrument input circuits.

5.2 Where the optional check of the input circuits is provided, the method of introducing code violations into the input digital signal shall be agreed. The violations shall be as defined in § 2 above.

6 Recorder output

6.1 An output signal may optionally be provided by the instrument to enable the status of the digital signal to be recorded externally in analogue and/or digital form.

6.2 For the analogue output, the signal shall vary corresponding to the measured result.

6.3 If the instrument has an analogue output, appropriate means for calibrating the external recorder shall be provided.

6.4 A possible arrangement relating the status of the digital input signal to the d.c. output signal is given in Table 2/O.161. The actual arrangement will depend upon the count period specified for the instrument (see § 4.2 above).

6.5 For the digital output of the measurement result, where provided, a parallel signal in binary coded decimal (BCD) form with transistor-transistor logic (TTL) levels shall be used.

7 Operating environment

The electrical performance requirements shall be met when operating at the climatic conditions as specified in Recommendation O.3, § 2.1.

H.T. [T2.161]
TABLE 2/O.161

Status	Deflection (mA or volts)	Tolerance (mA or volts)
No signal	0.5	—
Valid signal	5.5	± | .2
{ Violation rate ≥" 1 | (mu | 0^{D}lF261^{3} }	2.5	± | .2
{ Violation rate ≥" 1 | (mu | 0^{D}lF261^{4} }	2.5	± | .2
{ Violation rate ≥" 1 | (mu | 0^{D}lF261^{5} }	3.5	± | .2
{ Violation rate ≥" 1 | (mu | 0^{D}lF261^{6} }	3.5	± | .2
Single code violations	4.5	± | .2

TABLEAU 2/O.161 [T2.161], p. 7

Reference

[1] CCITT Recommendation *Physical/electrical characteristics of hierarchical digital interfaces* , Vol. III, Rec. G.703.

Recommendation O.162

EQUIPMENT TO PERFORM IN SERVICE MONITORING ON 2048 kbit/s SIGNALS

(Geneva, 1980, amended Melbourne, 1988)

1 General

1.1 This specification describes an instrument for performing in-service error tests on 2 Mbit/s signals having frame structures that are in accordance with Recommendation G.704 [1].

1.2 The instrument is required to monitor a 2048-kbit/s HDB3 encoded signal, display any inherent alarm condition in the signal and be capable of counting errors in the frame alignment signal.

1.3 The instrument may also, if so desired, count and display HDB3 code violations as a separate facility.

1.4 The instrument is required to monitor any cyclic redundancy check (CRC) procedure signals, in accordance with Recommendation G.704 [1], conveyed within the frame alignment signal, and time slot 0 (TSO) of frames not containing the frame alignment signal.

1.5 As an option the instrument may provide access to the information bits conveyed in any selected time slot.

1.6 *HDB3 decoding strategy*

When necessary, the received digital signal shall be decoded by the instrument in a manner such that, when sampling the signal, on recognition of 2 consecutive zeros (spaces) followed by a bipolar violation, the decoder shall substitute 4 consecutive zeros in place of the bipolar violation and the 3 preceding digits.

2 Input signal

2.1 *Interface*

The instrument shall be capable of operating with the interface at 2048 kbit/s corresponding to Recommendation G.703 [2], § 6.

2.2 *Input sensitivity*

2.2.1 The instrument is required to operate satisfactorily under the following input conditions.

2.2.1.1 Input impedances and levels in accordance with Recommendation G.703 [2].

2.2.1.2 The instrument shall also be capable of monitoring at protected test points on digital equipment. Therefore, a high impedance input and/or additional gain of 30 dB shall be provided to compensate for the loss at the monitoring points already provided on some equipment.

2.2.1.3 Additionally the instrument is required to operate satisfactorily, in both the terminated and monitor mode, when connected to an interface output in accordance with Recommendation G.703 [2] via a length of cable which can have an insertion loss of 0 dB to 6 dB at the half bit rate of the signal. The insertion loss of the cable at other frequencies will be proportional to $\sqrt{f}$.

2.3 *Input impedance*

2.3.1 The instrument shall have a return loss of better than 20 dB against a nonreactive 75/120/130-ohm resistor over a frequency range of 40 kHz to 2500 kHz.

2.4 *Signal input gating*

2.4.1 The instrument shall incorporate a timing recovery circuit, operated from the incoming digital signal, such that the instrument senses only the voltages which are present during a short gating period at the midpoint of each digit time slot.

2.5 *Input jitter tolerance*

2.5.1 The instrument shall be able to tolerate the lower limit of maximum tolerable input jitter specified in Recommendation G.823 [3].

3 Facilities

3.1 The instrument shall incorporate fault indications to meet the alarm strategies of equipments meeting Recommendation G.732 [4].

3.2 A possible fault indication plan is illustrated in § 3.3 below. All fault indicators are normally extinguished.

3.3 *Fault indication plan*

3.3.1 *Input signal failure*

A fault indication shall be given if more than 10 consecutive zeros are detected.

3.3.2 *Alarm indication signal (AIS)*

The instrument shall recognize a signal containing less than 3 zeros in a 2-frame period (512 bits) as a valid AIS signal and the appropriate indicator shall be lit.

The strategy for the detection of the presence of an AIS shall be such that the AIS is detectable even in the presence of a code violation rate of 1 in 10^3. However, a signal with all bits in the 1s state, except the frame alignment signal (FAS), shall not be mistaken for a valid AIS.

3.3.3 *Frame*

3.3.3.1 In the event of a loss of frame alignment, as defined in Recommendation G.706 [5], § 4, the instrument shall recognize the loss and the appropriate indicator shall be lit.

3.3.3.2 In the event of recovery of frame alignment, as defined in Recommendation G.706 [5], § 4, the indicator shall be extinguished.

Note — The instrument shall be able to synchronize to frames with or without CRC bits.

3.3.4 *Errors in the frame alignment signal*

3.3.4.1 The instrument shall have a means of indicating bit error rates, e.g. 1×10^{D}lF261^3, 1×10^{D}lF261^4, 1×10^{D}lF261^5 and illuminate the appropriate indicator.

The indication of bit error rates occurring in the received decoded signal and detected as incorrect frame alignment signals shall comply with the limits given in Table 1/O.162. The requirements in the table shall apply on the assumption that the average bit error rates are present for the whole of the counter measurement period.

H.T. [T1.162]

TABLE 1/O.162

Bit error rate indication	{	Illuminate	Extinguish
1 | (mu | 0 D lF261 3 1 | (mu | 0 D lF261 3 5 | (mu | 0 D lF261 4 1 | (mu | 0 D lF261 4 }	{		
50% within 0.3 s 5% within 0.3 s — }	{		
5% within 0.3 s — 95% within 0.3 s }			
1 | (mu | 0 D lF261 4 1 | (mu | 0 D lF261 4 5 | (mu | 0 D lF261 5 1 | (mu | 0 D lF261 5 }	{		
50% within 3 s 5% within 3 s — }	{		
5% within 3 s — 95% within 3 s }			
1 | (mu | 0 D lF261 5 1 | (mu | 0 D lF261 5 5 | (mu | 0 D lF261 6 1 | (mu | 0 D lF261 6 }	{		
50% within 30 s 5% within 30 s — }	{		
5% within 30 s — 95% within 30 s }			

Table 1/O.162 [T1.162] p.

3.3.4.2 It shall also be possible to count the sum of the errors indicated. The count capacity shall be 99 | 99. A separate indication shall be given if the count exceeds this figure.

3.3.5 *Multiframe*

3.3.5.1 In the event of a loss of multiframe alignment, as defined in Recommendation G.732 [4], § 5.2, the instrument shall recognize the loss and the appropriate indicator shall be lit.

3.3.5.2 In the event of recovery of multiframe alignment, as defined in Recommendation G.732 [4], § 5.2, the indicators shall be extinguished.

3.3.5.3 If time slot 16 is used for common channel signalling, the multiframe alignment signal is not present in a nominal input signal to the instrument. In this case it shall be possible to inhibit the loss of multiframe indicator in order to prevent false alarm indications.

3.3.6 *Distant alarm*

The instrument shall recognize the distant alarm condition as defined in Recommendation G.732 [4] (bit 3 of time slot 0 in frames alternate to those containing the frame alignment signal for at least 2 consecutive occasions and recognized within 4 consecutive occasions) and the appropriate indicator shall be lit.

3.3.7 *Distant multiframe alarm*

3.3.7.1 The instrument shall recognize the distant multiframe alarm condition as defined in Recommendation G.732 [4] (bit 6 of time slot 16, frame 0 for at least 2 consecutive occasions and recognized within 3 consecutive occasions) and the appropriate indicator shall be lit.

3.3.7.2 If time slot 16 is used for common channel signalling, bit 6 will be continuously in state 1. In this case it shall be possible to inhibit the distant multiframe alarm in order to prevent false alarm indications.

3.4 *Cyclic redundancy check procedure*

3.4.1 Where a cyclic redundancy check (CRC) procedure in accordance with Recommendation G.704 [1] is implemented within the 2 Mbit/s signal the instrument shall provide the features detailed in §§ 3.4.2, 3.4.3 and 3.4.4.

3.4.2 The instrument shall indicate the presence of CRC framing bits.

3.4.3 The instrument shall have a means of indicating bit error rates of 1×10^{D}lF261^{5}, 1×10^{D}lF261^{6} and 1×10^{D}lF261^{7} and shall cause the appropriate indicator to be illustrated under the conditions defined.

The indication of bit error rates occurring in the received decoded signal and detected by means of the CRC procedure information shall comply with the limits given in Table 2/O.162.

H.T. [T2.162]

TABLE 2/O.162

Bit error rate indication	{	Illuminate	Extinguish
1 | (mu | 0 D lF261 5 1 | (mu | 0 D lF261 5 5 | (mu | 0 D lF261 6 1 | (mu | 0 D lF261 6 }	{		
50% within 1 s 5% within 1 s — }	{		
5% within 1 s — 95% within 1 s }			
1 | (mu | 0 D lF261 6 1 | (mu | 0 D lF261 6 5 | (mu | 0 D lF261 7 1 | (mu | 0 D lF261 7 }	{		
50% within 10 s 5% within 10 s — }	{		
5% within 10 s — 95% within 10 s }			
1 | (mu | 0 D lF261 7 1 | (mu | 0 D lF261 7 5 | (mu | 0 D lF261 8 1 | (mu | 0 D lF261 8 }	{		
50% within 100 s 5% within 100 s — }	{		
5% within 100 s — 95% within 100 s }			

Table 2/O.162 [T2.162], p.

3.4.4 It shall also be possible to count the sum of errors indicated. The count capacity shall be 99 999. A separate indication shall be given if the count exceeds this figure.

3.5 *Code violation detection*

3.5.1 *Definition of an HDB3 code violation*

Two consecutive bipolar violations of the same polarity. This may not be the absolute number of errors.

3.5.2 When used as an HDB3 code violation detector the instrument shall incorporate an indicator to indicate the presence of a digital signal of correct amplitude and bit rate.

3.5.3 The code violation rate shall be indicated in the range 1 in 10^3 to at least 1 in 10^6. Indications of code violations occurring in the input signal and detected as defined in § 3.5.1 above, shall be determined by counting the number of code violations that occur during the period of at least 10^6 time slots.

3.5.4 It shall be possible to indicate the sum of the code violations. This facility will not be required at the same time as the code violation rate is being counted and displayed.

3.5.5 The count capacity shall be 99 | 99 and a separate indication shall be given if the count exceeds this figure.

3.6 *Performance indications*

As an option the instrument shall be capable of providing performance information in accordance with G.821 [6].

3.7 *Lamp lock — Lamp auto reset*

A facility shall be provided whereby the fault indication lamps either clear automatically when the fault condition clears or remain lit until a manual reset is operated.

3.8 *Time slot access*

As an option it shall be possible to access, at an external interface, the contents of any selected time slot, including time slot 16. An external interface meeting the requirements of a co-directional interface, as defined in Recommendation G.703 [2], is preferred.

4 Display

4.1 The counting sequence shall be started by operating a ‘‘start’’ control and shall be stopped by a ‘‘stop’’ control.

4.2 References to counters and displays being illuminated and extinguished does not imply that ‘‘light emitting’’ displays are essential.

4.3 The counter, and its display, shall be capable of being reset.

5 Alarm function check

A method of introducing fault conditions into the incoming digital signal, in order to check the correct functioning of the instrument, shall be considered.

6 Alarm output signal

As an option, an interface shall be provided to enable an external device, e.g. printer, to be connected to the instrument to allow recording of the status of the digital signal input to the instrument.

An interface in accordance with Recommendation V.24 [7] or V.28 [8], carrying suitably abbreviated, plain text messages in ASCII/T.50 [9] coded format according to the requirements of Recommendation V.4 [10] is preferred.

7 Operating environment

The electrical performance requirements shall be met when operating within the climatic conditions specified in Recommendation O.3, § 2.1.

References

[1] CCITT Recommendation *Synchronous frame structures used at primary and secondary hierarchical levels* , Vol. III, Rec. G.704.

[2] CCITT Recommendation *Physical/electrical characteristics of hierarchical digital interfaces* , Vol. III, Rec. G.703.

[3] CCITT Recommendation *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy* Vol. III, Rec. G.823.

[4] CCITT Recommendation *Characteristics of primary PCM multiplex equipment operating at 2048 kbit/s* , Vol. III, Rec. G.732.

[5] CCITT Recommendation *Frame alignment and CRC procedures relating to frames defined in Rec. G.704* , Vol. III, Rec. G.706.

[6] CCITT Recommendation *Error performance of an international digital connection forming part of an integrated digital network* , Vol. III, Rec. G.821.

[7] CCITT Recommendation *List of definitions for interchange circuits between data terminal equipment and data circuit-terminating equipment* , Vol. VIII, Rec. V.24.

[8] CCITT Recommendation *Electrical characteristics or unbalanced double-current interchange circuits* , Vol. VIII, Rec. V.28.

[9] CCITT Recommendation *International Alphabet No. 5* , Vol. VII, Rec. T.50.

[10] CCITT Recommendation *General structure of signals of International Alphabet No. 5 code for character oriented data transmission over public telephone networks* , Vol. VIII, Rec. V.4.

Recommendation O.163

EQUIPMENT TO PERFORM IN-SERVICE MONITORING ON 1544 kbit/s SIGNALS

(Melbourne, 1988)

1 General

1.1 This specification describes frame alignment signal monitoring equipment for 1544 kbit/s frame structures that are in accordance with Recommendation G.704 [1]. This equipment is intended to monitor 12-frame multiframe (superframe format — SF) or 24-frame multiframe (extended superframe format — ESF) structures having either AMI or B8ZS line codes as defined in § 2 of Recommendation G.703 [2].

1.2 This equipment shall provide the following capabilities:

a) monitor and display the error performance of the frame alignment signal;

b) detect and accumulate the counts of occurrences of loss of frame alignment;

c) measure and display the error performance of 24-frame multiframe signals by monitoring the cyclic redundancy check (CRC-6) bits and performing a CRC-6 procedure in accordance with Recommendation G.704 [1] and as described below;

d) detect and display the various alarm or fault conditions including loss of signal, loss of frame alignment, and other alarm conditions indicated by specific bit patterns.

1.3 The equipment may optionally provide the following additional capabilities:

a) detect and display the code violations in the 1544 kbits signal in accordance with Recommendation O.161;

b) provide an external interface for extracting the information bits conveyed in any selected channel time slot;

c) provide an external interface for extracting the 4 kbit/s data link bits defined in the 24-frame multiframe structure;

d) provide an external interface for extracting the signalling bits in the 12-frame and 24-frame structures.

2 Input requirements

2.1 *Interface*

The specification of protected monitoring points is under study in SG XV and SG IV.
The monitoring equipment shall be capable of operating with a test load impedance at a 1544 kbit/s interface as defined in § 2 of Recommendation G.703 [2]. It shall also be capable of operating when connected to protected monitoring points (see also Recommendation G.772 [3]).

2.2 *Input impedance*

2.2.1 *Input impedance* | (resistive) 100 ohms

2.2.2 *Return loss (20 kHz to 1600 kHz)* > 20 dB

2.3 *Input sensitivity*

As a minimum, the monitoring equipment shall operate properly in the line terminating mode over the range of bit rates, pulse shapes and signal levels defined in § 2 of Recommendation G.703 [2]. It shall also be equipped with an additional gain to compensate for the isolation loss incurred at protected monitoring points (see also Recommendation G.772 [3]). A signal level indicator, or other means, shall be provided for the proper adjustment of input sensitivity.

2.4 *Input jitter tolerance*

The monitoring equipment shall be able to tolerate input jitter specified in Table 2/G.824 [4] without degradation of measuring accuracy.

2.5 *Input line codes*

The monitoring equipment is intended for use with both AMI and B8ZS line codes. The instrument shall have the capability to select either AMI or B8ZS, through a switch or other appropriate means. The instrument should indicate when it is receiving B8ZS when switched to the AMI mode, and vice versa.

3 Detection, measurement, and indication requirements

3.1 *Detection and indication of fault conditions*

3.1.1 *Loss of line signal*

Under study.

3.1.2 *Loss of frame alignment*

The equipment shall recognize the loss of frame alignment as defined in Recommendation G.706 [5], and an appropriate indication shall be given.

3.1.3 *Recovery of frame alignment*

The procedure for determining recovery of frame alignment shall be in accordance with Recommendation G.706 [5]. When frame recovery is complete, the indication of loss of frame alignment shall cease.

3.1.4 *Alarm indication signal (AIS) from an upstream failure*

The equipment shall recognize the presence of an alarm indication signal (AIS) indicating an upstream failure, and an appropriate indication shall be given. The binary equivalent of the AIS corresponds to an all ones signal. The strategy for the detection of the presence of an AIS shall be such that with a high probability, it is detected even in the presence of a code violation ratio of 1 in 1000.

3.1.5 *Distant alarm indication signal (DAIS)*

The equipment shall recognize the presence of distant alarm indication signal as defined in Recommendation G.733 [6], § 4.2.4 for both 12-frame and 24-frame multiframe signals, and an appropriate indication shall be given. The strategy for the detection of the presence of this distant alarm indication signal shall be such that with a high probability, it is detected even in the presence of a code violation ratio of 1 in 1000.

3.2 *Frame alignment signal (FAS) error performance measurements*

3.2.1 *Count of errored seconds*

The equipment shall be capable of counting the number of one second intervals in which one or more errors occur in the FAS bits associated with the 12-frame or 24-frame structures as defined in Recommendation G.704 [1]. The number of errored seconds in a selectable time period (see § 4.1) shall be counted and displayed. The equipment shall establish one-second intervals independent of the occurrence of errors.

3.2.2 *Count of errors*

The equipment shall be capable of counting the number of FAS bit errors occurring in a selectable time period (see § 4.1).

3.3 *CRC-6 error performance monitoring*

3.3.1 *Count of errored seconds*

The equipment shall be capable of counting the number of one-second intervals in which one or more CRC-6 violations are detected in 24-frame multiframe signals using the CRC-6 procedure defined in Recommendation G.704 [1] and G.706 [5]. The number of errored seconds in a selectable time period shall be counted and displayed. The equipment shall establish one-second intervals independent of the occurrence of errors.

3.3.2 *Performance indications*

As an option the instrument shall be capable of providing performance information in accordance with Recommendation G.821 [7].

3.3.3 *Estimate of bit-error-ratio*

This equipment shall optionally be capable of providing an estimate of the bit-error-ratio performance of 24-frame multiframe signals in the range 10^{D}lF261^{4} to 10^{D}lF261^{7} by detecting CRC-6 violations. In performing this measurement, it shall be assumed that only one bit-error has occurred each time a CRC-6 violation is detected. It is noted that this may not be an accurate estimate since more than one bit-error may occur within a 24-frame multiframe, due to the bursty nature of error occurrences.

The time interval for each bit-error-ratio measurement that is within the required range of the equipment shall be sufficiently long to include at least ten CRC violations.

3.3.4 *Count of errors*

The equipment shall also be capable of counting the number of CRC-6 violations occurring in a selectable time period (see § 4.1).

3.4 *Loss of frame-alignment count*

The equipment shall be capable of counting the occurrences of loss of frame alignment over a selectable time period (see § 4.1). Error counters shall be disabled during intervals of loss of frame alignment.

3.5 *Measurement of code violations*

If the measurement of 1544 kbit/s code violations is included, the equipment shall meet the requirements of Recommendation O.161.

3.6 *Channel time slot access*

As an option, receiving access may be provided to a selected 64 kbit/s channel at an external interface. An interface meeting the requirements of a co-directional interface output port defined in Recommendation G.703 [2], is preferred. In addition a centralized clock interface as defined in Recommendation G.703 [2] may be provided.

3.7 *4 kbit/s data link access*

Under study.

3.8 *Signaling bit access*

Under study.

4 Control and display requirements

4.1 *Measurement timer*

A measurement interval timer shall be provided for the convenience of the user when counting errors. The timer shall be adjustable from 5 minutes to 24 hours in steps of one minute or continuous. Manual ‘‘start’’ and ‘‘stop’’ controls shall also be provided.

4.2 *Count registers*

The count registers shall have a capacity of at least 99999. A separate means for indicating overflow shall be provided. Each of the registers shall be capable of being independently reset. A separate register shall be provided for each parameter or condition listed in §§ 3.1 through 3.4.

4.3 *Selection of multiframe structure*

A control shall be provided to permit a user to select whether the 12-frame or 24-frame multiframe structure is being monitored. As an option the equipment may automatically sense and display whether the signal being monitored is a 12-frame, 24-frame or neither multiframe structure.

4.4 *Lock/reset of displays*

For each of the fault condition indications given in § 3.1 means shall be provided whereby the display will remain visible until a manual reset is operated.

5 Monitoring equipment self diagnostics

5.1 As an option, an internal self diagnostic system to check for correct functioning of the instrument, shall be provided.

6 Interface for remote control and measurement results

6.1 As an option, an interface shall be provided for remote control of the frame signal monitoring equipment, and transmission of measurement results. If provided, the interface bus shall comply with one of the following:

a) ANSI/IEEE Std 488-1978 [8]

b) IEC Publication 625 [9]

c) ANSI/EIA-232-D-1986 [10].

7 Operating environment

The electrical performance requirements shall be met when operating under climatic conditions as specified in Recommendation O.3, § 2.1.

References

[1] CCITT Recommendation *Synchronous frame structures used at primary and secondary hierarchical levels* , Vol. III, Rec. G.704.

[2] CCITT Recommendation *Physical/electrical characteristics of hierarchical digital interfaces* , Vol. III, Rec. G.703.

[3] CCITT Recommendation *Digital protected monitor points* , Vol. III, Rec. G.772.

[4] CCITT Recommendation *The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy* , Vol. III, Rec. G.824.

[5] CCITT Recommendation *Frame alignment and cyclic redundancy check (RCR) procedures relating to basic frame structures defined in Recommendation G.704* , Vol. III, Rec. G.706.

[6] CCITT Recommendation *Characteristics of primary PCM multiplex equipment operating at 1544 kbit/s* , Vol. III, Rec. G.733.

[7] CCITT Recommendation *Error performance of an international digital connection forming part of an integrated service digital network* , Vol. III, Rec. G.821.

[8] ANSI/IEEE Std 488-1978, *IEEE standard digital interface for programmable instrumentation* .

[9] IEC Publication 625 *An interface system for programmable measuring instruments (byte serial, bit parallel)* .

[10] ANSI/EIA-232-D-1986 *Interface between data terminal equipment and data circuit terminating equipment employing serial binary data interexchange* .

Recommendation O.171

TIMING JITTER MEASURING EQUIPMENT FOR DIGITAL SYSTEMS

(Geneva, 1980; amended Malaga-Torremolinos, 1984 and Melbourne, 1988)

1 Introduction

1.1 *General*

1.1.1 The instrumentation specified below will be used to measure timing jitter on digital equipment. This instrumentation, which consists of a jitter measuring circuit and a test signal source, is shown in a general form in Figure 1/O.171. While essential requirements are given for the instrumentation, the realization of the equipment configuration is not covered and should be given careful consideration by the designer and user. An error-ratio meter may also be required for certain types of measurements.

See the Supplement No. 3.8 at the end of this fascicle.

Figure 1/O.171, p.

1.1.2 Certain requirements in this specification are provisional and are still under study. These are individually indicated.

1.1.3 It is recommended that Recommendation G.823 [2] be read in conjunction with this Recommendation.

1.2 *Interfaces*

1.2.1 The instrumentation shall be capable of operating at one or more of the following bit rates and corresponding interface characteristics as described in the appropriate paragraphs of Recommendation G.703 [1]. However, for all bit rates the signal applied to the input of the jitter measuring circuit should be a nominal rectangular pulse. Other signal shapes may produce intersymbol interference thus affecting measurement accuracy.

a) 64 kbits,

b) 1544 kbit/s,

c) 6312 kbit/s,

d) 2048 kbit/s,

e) 8448 kbit/s,

f) 32 | 64 kbit/s,

g) 44 | 36 kbit/s,

h) 34 | 68 kbit/s,

i) 139 | 64 kbit/s.

References to 64 kbit/s relate to the codirectional interface. Limits for other 64 kbit/s interfaces are under study.

1.2.2 As an option the jitter measuring circuit shall be capable of measuring jitter at a clock output port when such an access is provided on digital equipment.

1.3 *Interface impedances*

1.3.1 The jitter measuring circuit and signal source shall have a return loss better than 20 dB under the conditions listed in Table 1/O.171.

H.T. [T1.171]
TABLE 1/O.171
Return loss test conditions

Bit rate (kbit/s)	Test conditions	
| 64	120 ohms, nonreactive	3 kHz to 300 KHz
1 | 44	100 ohms, nonreactive	20 kHz to 1.6 MHz
2 | 48	75/120/130 ohms, nonreactive	40 kHz to 2.5 MHz
6 | 12	75/110 ohms, nonreactive	100 kHz to 6.5 MHz
8 | 48	75 ohms, nonreactive	100 kHz to 10 MHz
32 | 64	75 ohms, nonreactive	500 kHz to 40 MHz
34 | 68	75 ohms, nonreactive	500 kHz to 40 MHz
44 | 36	75 ohms, nonreactive	500 kHz to 50 MHz
139 | 64	75 ohms, nonreactive	7 kHz to 210 MHz

Table 1/O.171 [T1.171], p.

2 Test signal source

Tests of digital equipment may be made with either a jittered or a non-jittered digital signal. This will require the pattern generator, clock generator and modulation source shown in Figure 1/O.171.

2.1 *Modulation source*

The modulation source, testing in conformance with the Series G.700 Recommendations, may be provided within the clock generator and/or pattern generator or it may be provided separately. In this Recommendation it is assumed that the modulation source is sinusoidal.

In the case of 1544 kbit/s, the signal source shall have the following return loss: 20 kHz to 500 kHz ≥" 14 dB and 500 kHz to 1.6 MHz ≥ 16 dB.

2.2 *Clock generator*

2.2.1 It shall be possible to phase modulate the clock generator from the modulation source and to indicate the peak-to-peak phase deviation of the modulated signal.

The generated peak-to-peak jitter and the modulating frequencies shall meet the requirements of Figure 2/O.171 and Table 2/O.171.

2.2.2 The modulating input sensitivity of the clock generator shall be at least:

a) 2 volts peak-to-peak into 600 ohms for bit rates up to and including 8448 kbit/s,

b) 1 volt peak-to-peak into 75 ohms for bit rates up to and including 139 | 64 kbit/s.

2.2.3 The minimum output of the modulated clock signal and the external timing reference signal shall be 1 volt peak-to-peak into 75 ohms.

2.2.4 *Accuracy of the clock generator*

Accuracy requirements are still under study.

2.3 *Pattern generator*

The jitter measuring circuit will normally be used with any suitable pattern generator providing the following facilities.

Note — When test signals are applied to the input of a digital demultiplexer, they must contain the frame alignment signal and justitication control bits. Other measurement techniques are available which do not require the addition of the frame alignment signal or justification control bits.

2.3.1 *Patterns*

The pattern generator shall be capable of providing the following patterns:

Note — Longer pseudorandom patterns may be necessary for jitter measurements on digital line systems and digital line sections [1].

2.3.1.1 For use at bit rates of 64 kbit/s, a pseudorandom pattern of $2^{11} - 1$ bit length corresponding to Recommendation O.152. Encoding in accordance with Recommendation G.703 [1], § 1.2.1.

2.3.1.2 For use at bit rates of 1544 kbit/s 6312 kbit/s and 44 736 kbit/s, pseudorandom patterns of $2^{15} - 1$, $2^{20} - 1$, $2^{23} - 1$ bit length corresponding to Recommendation O.151, § 2.

Note — Definition of the $2^{20} - 1$ pseudorandom pattern is under study.

2.3.1.3 For use at bit rates of 2048 kbit/s, 8448 kbit/s and 32 064 kbit/s, a pseudorandom pattern of $2^{15} - 1$ length corresponding to Recommendation O.151, § 2.1.

2.3.1.4 For use at bit rates of 34 | 68 kbit/s and 139 | 64 kbit/s, a pseudorandom pattern of $2^{23} - 1$ bit length corresponding to Recommendation O.151, § 2.2.

2.3.1.5 For use at all bit rates, a 1000 1000 repetitive pattern.

2.3.1.6 As an option and for use at all bit rates:

a) two freely programmable 8-bit patterns capable of being alternated at a low rate (e.g. from 10 Hz to 100 Hz),

b) a freely programmable 16-bit pattern.

2.3.2 *Generation errors*

The detailed specification of pattern generator parameters, to be compatible with the jitter measuring circuit specification, is under study.

Figure 2/O.171 p. 12

H.T. [T2.171]
TABLE 2/O.171
Generated jitter amplitude versus jitter frequency

Bit rate (kbit/s) { A 1: Minimum value of generated jitter from *f* 0 to *f* 2 } { A 2: Minimum value of generated jitter from *f* 3 to *f* 4 }		
| 64	5.0 UI from 2 Hz to 600 Hz	0.5 UI from 6 kHz to 10 kHz
1 | 44	10.0 UI from 2 Hz to 200 Hz	0.5 UI from 4 kHz to 40 kHz
2 | 48	10.0 UI from 2 Hz to 2400 Hz	0.5 UI from 45 kHz to 100 kHz
6 | 12	10.0 UI from 2 Hz to 1600 Hz	0.5 UI from 32 kHz to 160 kHz
8 | 48 0.5 UI from 8.5 kHz to 400 kHz }	10.0 UI from 2 Hz to 400 Hz	{
32 | 64	10.0 UI from 2 Hz to 1600 Hz	0.5 UI from 32 kHz to 800 kHz
34 | 68	10.0 UI from 2 Hz to 1000 Hz	0.5 UI from 20 kHz to 800 kHz
44 | 36 0.5 UI from 100 kHz to 4500 kHz }	16.0 UI from 2 Hz to 3200 Hz	{
139 | 64 0.5 UI from 10 kHz to 3500 kHz }	10.0 UI from 2 Hz to 500 Hz	{
8 | 48 (low Q) 0.5 UI from 200 kHz to 400 kHz }	10.0 UI from 2 Hz to 10.7 kHz	{

Note 1 to Figure 2/O.171 and Table 2/O.171 — Amplitude of jitter specified as peak-to-peak value in unit intervals (UI).

Note 2 to Figure 2/O.171 and Table 2/O.171 — *f* 1 lies between *f* 0 and *f* 2 (see Figure 3/O.171 and Table 3/O.171). It is not defined here since it is not significant in the context of the requirements of the clock generator.

3 Jitter measuring circuit

3.1 *Input sensitivity*

The jitter measuring circuit is required to operate satisfactorily under the following input conditions:

a) The specification for equipment output ports listed in Recommendation G.703 [1].

b) The jitter measuring circuit shall also be capable of measuring at protected test points on digital equipment. Therefore, an additional gain of 30 dB (40 dB) shall be provided to compensate for the flat loss at the monitoring points already provided on some equipment.

Note 1 — As an option for instrumentation operating at an interface of 1544 kbit/s the additional gain, where provided, shall be 40 dB.

Note 2 — The influence of the additional gain of 40 dB and of frequency dependent cable loss on the measurement accuracy is under study.

3.2 *Measurement ranges*

3.2.1 The jitter measuring circuit shall be capable of measuring peak-to-peak jitter optional but for reasons of compatibility the jitter amplitude/jitter frequency response of the jitter measuring circuit shall meet the requirements of Figure 3/O.171 and Table 3/O.171 where f_1 to f_4 are the frequencies defining the jitter frequencies to be measured.

3.2.2 When measuring peak-to-peak jitter it shall also be possible to count the number of occasions and the period of time for which a given selectable threshold of jitter is exceeded. It shall be possible to record these events by means of an external counter, or an internal counter as an option.

3.2.3 It shall be possible to set the threshold of § 3.2.2 at any selected measurement value within the measuring range of the jitter measuring circuit.

3.2.4 As an option, the jitter measuring circuit shall be capable of measuring r.m.s. jitter. In such cases it shall be possible to measure 3.0 unit intervals (UI) at jitter frequencies up to f_2, and 0.15 UI at jitter frequencies from f_3 to f_4 of Figure 3/O.171 and Table 3/O.171, the measurement ranges being optional.

3.2.5 Where the option in § 3.2.4 is not provided, the analogue output can be used to make r.m.s. measurements with an external meter.

Figure 3/O.171, p.

H.T. [T3.171]

TABLE 3/O.171

Measured jitter amplitude versus jitter frequency

Bit rate (kbit/s) A 1: Maximum value of jitter to be measured from *f* 1 to *f* 2 } A 2: Maximum value of jitter to be measured from *f* 3 to *f* 4 }	{ {	
| 64	5.0 UI from 20 Hz to 600 Hz	0.5 UI from 6 kHz to 10 kHz
1 | 44	10.0 UI from 10 Hz to 200 Hz	0.3 UI from 7 kHz to 40 kHz
2 | 48	10.0 UI from 20 Hz to 2400 Hz	0.5 UI from 45 kHz to 100 kHz
6 | 12	10.0 UI from 10 Hz to 1600 Hz	0.5 UI from 32 kHz to 160 kHz
8 | 48 0.5 UI from 8.5 kHz to 400 kHz }	10.0 UI from 20 Hz to 400 Hz	{
32 | 64	10.0 UI from 60 Hz to 1600 Hz	0.5 UI from 32 kHz to 800 kHz
34 | 68 10.0 UI from 100 Hz to 1000 Hz }	{ 0.5 UI from 20 kHz to 800 kHz	
44 | 36 0.5 UI from 100 kHz to 4500 kHz }	16.0 UI from 10 Hz to 3200 Hz	{
139 | 64 0.5 UI from 10 kHz to 3500 kHz }	10.0 UI from 200 Hz to 500 Hz	{
8 | 48 (low Q) 10.0 UI from 20 Hz to 10.7 kHz }	{ 0.5 UI from 200 kHz to 400 kHz	

Note to Figure 3/O.171 and Table 3/O.171 — Amplitude of jitter specified as peak-to-peak value in unit intervals (UI).

Table 3/O.171 [T3.171], p.

3.3 *Measurement bandwidths*

3.3.1 The basic jitter measuring circuit shall contain filters to limit the band of the jitter frequencies to be measured at the various bit rates. Additional filters shall be provided to further limit the bandwidth for the measurement of specified jitter spectra as defined in the Series G.700 Recommendations and for other uses. These additional filters may be either internal or external to the jitter measuring circuit. The filters are to be connected between the phase detector and the measuring device. The bandwidth of the jitter measuring circuit and the filters shall be in accordance with Table 4/O.171.

3.3.2 *Frequency response of jitter measuring circuit and filters*

The response of all filters within the passband shall be such that the accuracy requirements of the jitter measuring circuit are met.

At frequencies below the lower 3-dB point, the attenuation of the highpass filtration shall rise with a value greater than, or equal to, 20 dB per decade.

At frequencies above the upper 3-dB point the attenuation of the lowpass filtration shall rise with a value greater than, or equal to, 60 dB per decade.

However, the maximum attenuation of the filters shall be at least 60 dB.

Note — The effect of nonsinusoidal jitter on the requirements for the filters is still under study.

H.T. [T4.171]

TABLE 4/O.171

Jitter measurement bandwidths and highpass filter cutoff

frequencies

Bit rate (kbit/s)	Jitter measurement bandwidth {		{		{	
	f 1 (Hz) Highpass filter No. 1	*f* 4 (kHz) Highpass filter No. 2	{			
| 64	2	20	10	20	20 Hz	3 kHz
1 | 44	2	10	40	80	10 Hz	8 kHz
2 | 48	2	20	100	200	20 Hz	700 Hz 18 kHz
6 | 12	2	10	160	320	10 Hz 60 Hz	24 kHz 32 kHz
8 | 48	2	20	400	800	20 Hz	3 kHz 80 kHz
32 | 64	2	60	800	1600	60 Hz	160 kHz
34 | 68	2	100	800	1600	100 Hz	10 kHz
44 | 36	2	10	4500	9000	10 Hz	900 kHz
139 | 64	2	200	3500	7000	200 Hz	10 kHz

Note 1 — The accuracy of the instrument is specified between frequencies *f* 1 and *f* 4.

Note 2 —Two values are specified for highpass filter No. 1 at 6312 kbit/s and highpass filter No. 2 at 2048 kbit/s, 6312 kbit/s and 8448 kbit/s.

Table 4/O.171 [T4.171], p.

3.4 *Measurement accuracy*

3.4.1 *General*

The measuring accuracy of the jitter measuring circuit is dependent upon several factors such as fixed intrinsic error, frequency response and pattern-depending error of the internal reference timing circuits. In addition there is an error which is a function of the actual reading.

The total error at 1-kHz jitter frequency (excluding the error due to frequency response) shall be less than

± | % of reading ± | ± Y

where X is the fixed error of Table 5/O.171 and Y an error of 0.01 UI p-p (0.002 UI | dr\d.\dm\d.\ds\d.) which applies if internal timing extraction is used.

3.4.2 *Fixed error*

For the system bit rates and for the indicated test sequences the fixed error of the jitter measuring circuit shall be as listed in Table 5/O.171 when measured at any jitter frequency between f_1 and f_4 of Figure 3/O.171.

3.4.3 *Error at other frequencies*

At jitter frequencies between f_1 and f_4 other than 1 kHz, the error additional to that defined in § 3.4.1 above shall be as listed in Table 6/O.171.

Note — The limits of measuring accuracy of the jitter measuring circuit given in § 3.4 are provisional and are still under study.

H.T. [T5.171]

TABLE 5/O.171

Fixed error in jitter measurements

Bit rate (kbit/s)	{					
	1000 1000	Pseudorandom | ua)	All ones or clock input	p-p	r.m.s.	p-p
| 64	< 0.005	< 0.002	< 0.025	< 0.004	< 0.004	< 0.001
1 | 44	< 0.005	< 0.002	< 0.025	< 0.004	< 0.004	< 0.001
2 | 48	< 0.005	< 0.002	< 0.025	< 0.004	< 0.004	< 0.001
6 | 12	< 0.005	< 0.002	< 0.025	< 0.004	< 0.004	< 0.001
8 | 48	< 0.005	< 0.002	< 0.025	< 0.004	< 0.004	< 0.001

Tableau 5/O.171 [T5.171], p. 17

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H.T. [T6.171]

TABLE 6/O.171

Frequency response error

Bit rate (kbit/s)	Measurement bandwidth		{
	f 1 (Hz)	*f* 4 (kHz)	
| 64 ± | % 20 Hz to 600 Hz ± | % 600 Hz to 10 kHz }	20	10	{
1 | 44 ± | % *f* 1 to 1 kHz; ± 2% to *f* 4 }	10	40	{
2 | 48 ± | % *f* 1 to *f* 4 }	20	100	{
6 | 12 ± | % *f* 1 to 1 kHz; ± 2% to *f* 4 }	10	160	{
8 | 48 ± 2% *f* 1 to 300 kHz ± 3% 300 Hz to *f* 4 }	20	400	{
32 | 64	60	800	± 2% 60 Hz to 300 kHz
34 | 68 ± 3% 300 kHz to *f* 4 }	100	800	{
44 | 36 ± 4% 10 Hz to 200 Hz ± 2% 200 Hz to 300 kHz ± 3% 300 kHz to 1 MHz ± 5% 1 MHz to 3 MHz ± 10% > 3 MHz } 139 | 64	10 200	4500 3500	{

Tableau 6/O.171 [T6.171], p. 18

3.5 *Additional facilities*

3.5.1 *Analogue output*

The jitter measuring circuit shall provide an analogue output signal to enable measurements to be made externally to the jitter measuring circuit.

3.5.2 *Reference timing signal*

A reference timing signal for the phase detector is required. For end-to-end measurements it may be derived in the jitter measuring circuit from any input pattern. For loop-measurements it may be derived from a suitable clock source.

4 Operating environment

The electrical performance requirements shall be met when operating at the climatic conditions as specified in Recommendation O.3, § 2.1.

References

[1] CCITT Recommendation *Physical/electrical characteristics of hierarchical digital interfaces* , Vol. III, Rec. G.703.

[2] CCITT Recommendation *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy* , Vol. III, Rec. G.823.