



# CLIPPER CPU

**54-30158-03**  
**54-30158-05**

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## ★ 54-30158-03

- 500Mhz CPU module
- 4Mb Cache w/Motorola 5ns Late Write SRAMs

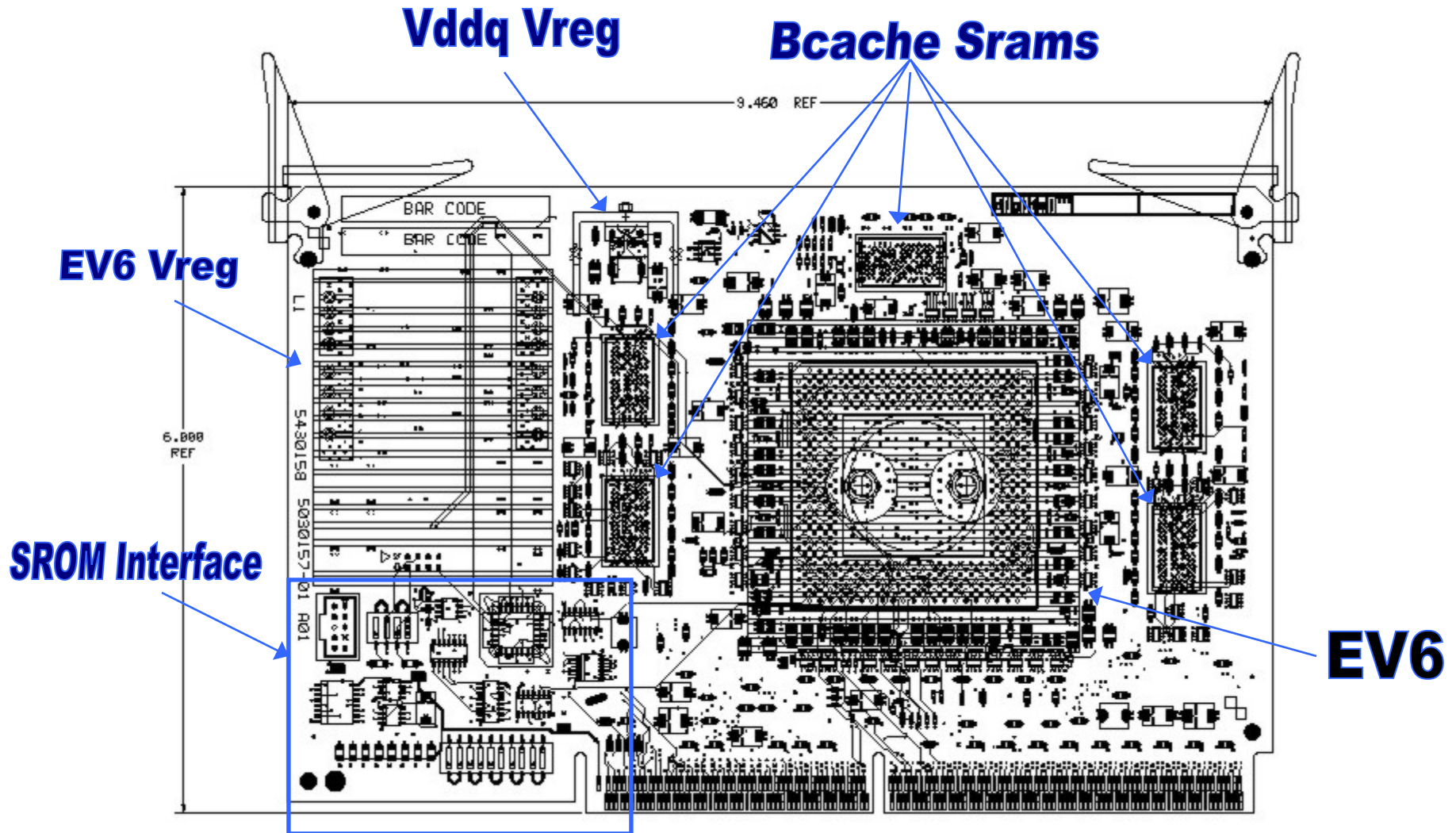
## ★ 54-30158-05

- 500Mhz CPU module
- 4Mb Cache w/IBM or Samsung 5ns Late Write SRAMs

- ⇒ Single EV6 processor per card with 500Mhz EV6 processor
- ⇒ 4mb 200MHz Cache using 5ns HSTL Late Write SRAMs
- ⇒ On-board Regulators:
  - EV6 Core voltage generated from 5V supply.
  - SRAM Vddq voltage generated from 3V supply.
- ⇒ EV6 Regulator Power Fail Detection
- ⇒ SROM / SPORT connector port for ease of diagnose and debug
- ⇒ I2C bus
  - EEPROM for module/error information storage including:
    - ◇ Module Serial number
    - ◇ Cache size
    - ◇ EV6 core voltage, OVP and UVP settings
    - ◇ VTERM and CTERM nominal setting and the min and max allowed settings.
    - ◇ Error information relevant to the module.
  - On-board temperature sensor

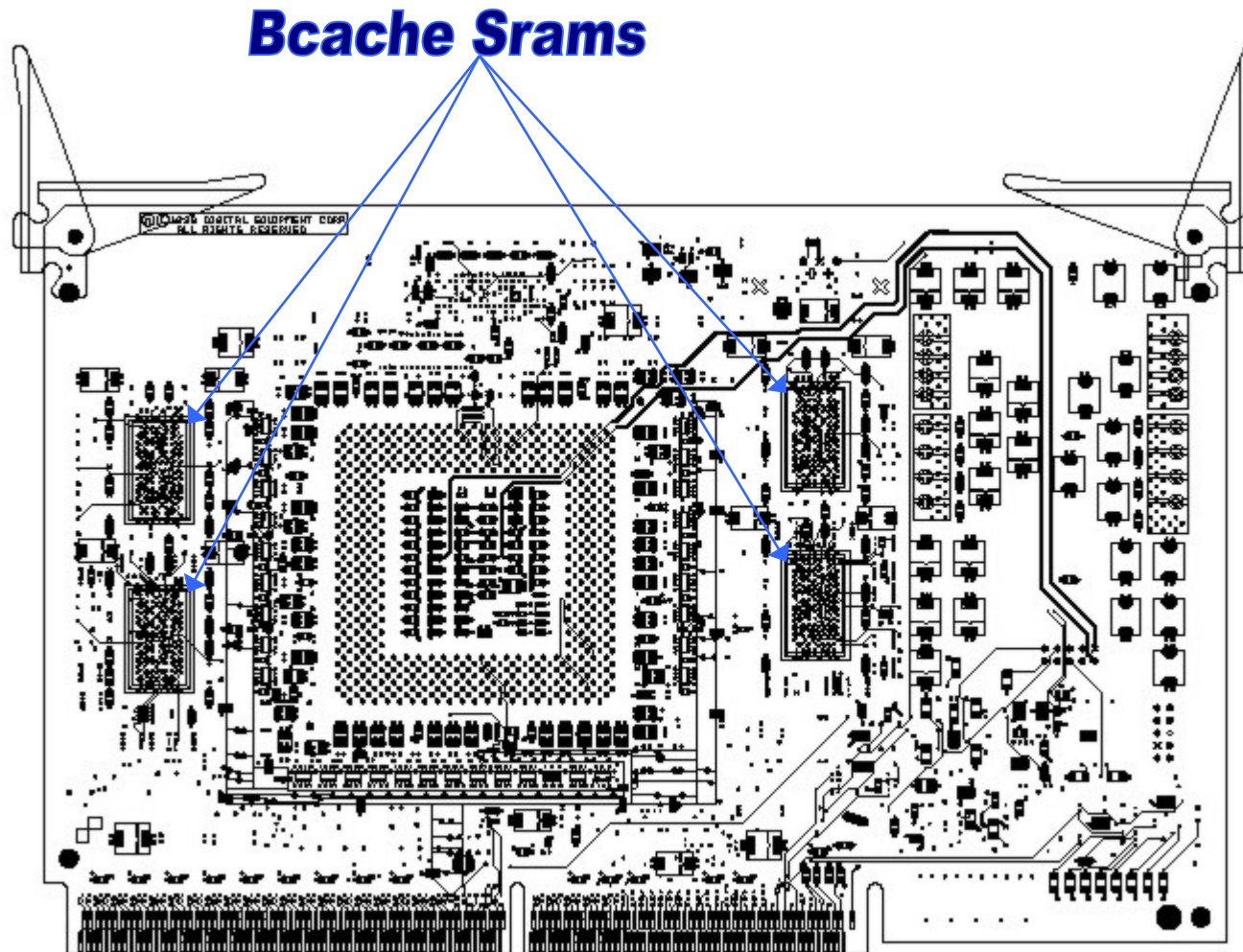
# CPU Module

## Side 1 View



# CPU Module

Side 2 View



- **Voltage checks**

- The output of both on-board regulators is monitored by the RMC
- On-board voltage checks
  - The EV6 Core voltage Regulator has built-in OVP.
  - The VDDQ Regulator has external OVP/UVF sensing.
  - A PAL monitors the above signals and deasserts CPU\_POK\_H if the voltage is out of range.
- Regulator controls
  - The RMC controls the enables for both regulators and determines when they will turn on and off.
  - The EV6 regulator voltage is set by a 4 bit input determined by populating/depopulating pulldown resistors.
  - The 1.5V VDDQ regulator output is fixed.
- Split “VTERM” Rails. CTERM for SYSDATIN and SYSADDIN clocks and VTERM for the rest of the System Interface. (OUTCLK pullups are also on CTERM but are located on the CSB).
  - CPU in slot 0 determines what value VTERM and CTERM will be for ALL CPUs.
  - On-board resistors and capacitors make up a portion of the VTERM and CTERM regulator's (located on the CSB) Trim and OVP circuits.

- **SROM / SPORT Interface**

- Both interfaces are available via the same connector on the CPU
- This is the standard SROM interface we've used since EV4
- Wim Lemmers (NGO) defined the SPORT interface needs. SPORT provides a connection to a PC for down-loading SROM code from the PC instead of the System SROM.

- **Heat Sink Temperature**

- EV6 Temp very dependent upon cooling and speed of operation
- During normal operation it should be fairly warm to the touch.
  - If it's cold it's not running
  - if it's too hot to touch it's either bad or the fan is dead