

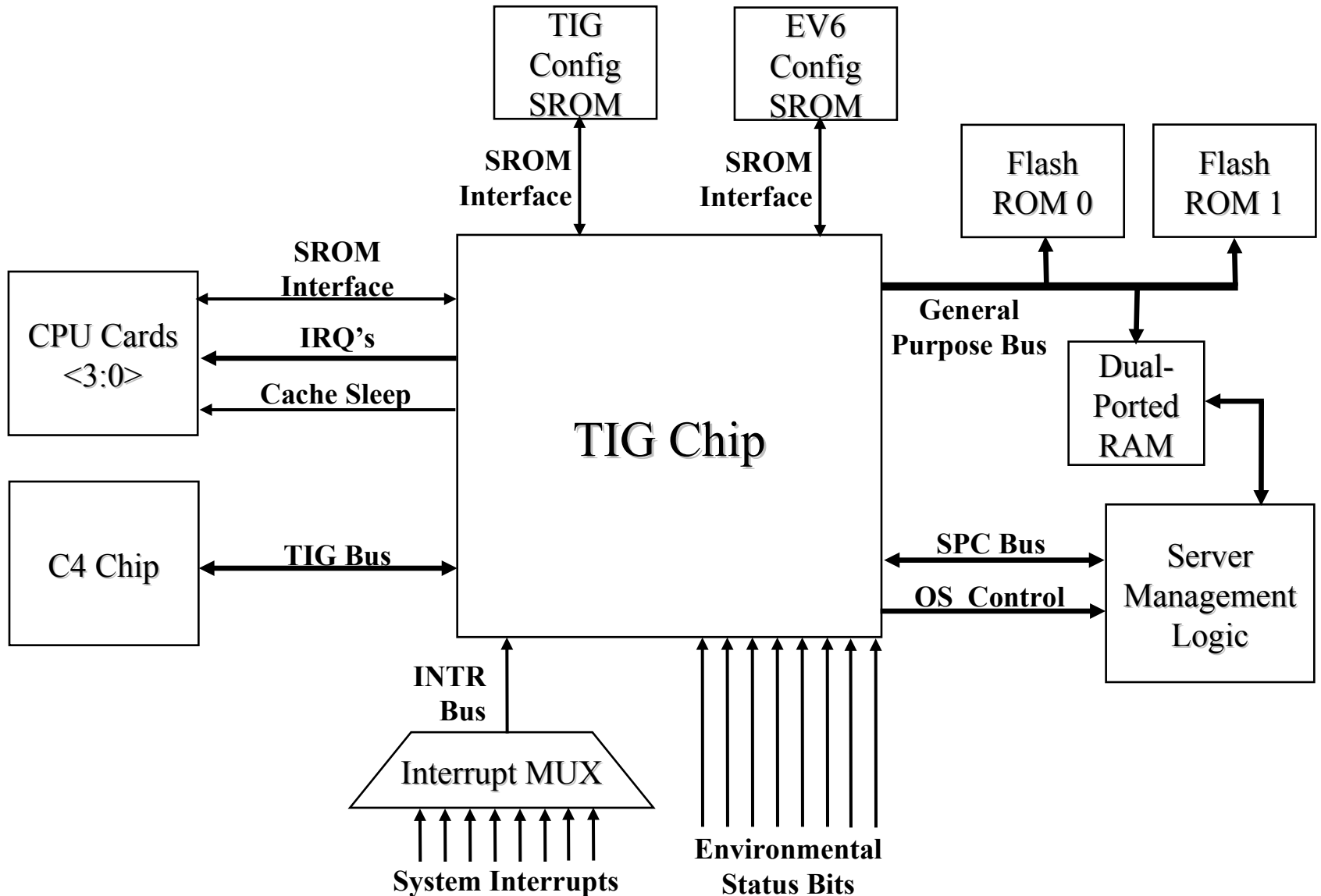


# Clipper TIG Chip

Presenter: Steve Baka

- **Receives interrupts from system interrupt mux and forwards them to the C4-Chip via the TIG bus.**
- **Latches IRQ's<3:0> from the C-chip via the TIG bus and forwards them to the EV6's.**
- **Provides a set of 8-bit internal registers used for:**
  - monitoring environmental status information
  - interprocessor communication
  - modifying system clock speeds
  - regulating EV6 power-up and configuration
  - system power down and putting cache to sleep
- **An 8-bit general purpose bus that provides access to:**
  - two 1MB Flash RAM's used containing firmware code (i.e., console)
  - one 16kB dual-ported RAM (DPR) used for communication with the server management corner.
- **A set of SROM data, output enable, and clock lines for each CPU that are used for EV6 configuration at power-ups/resets**
- **Provides interfaces for firmware and the OS to communicate with the Remote Server management corner**

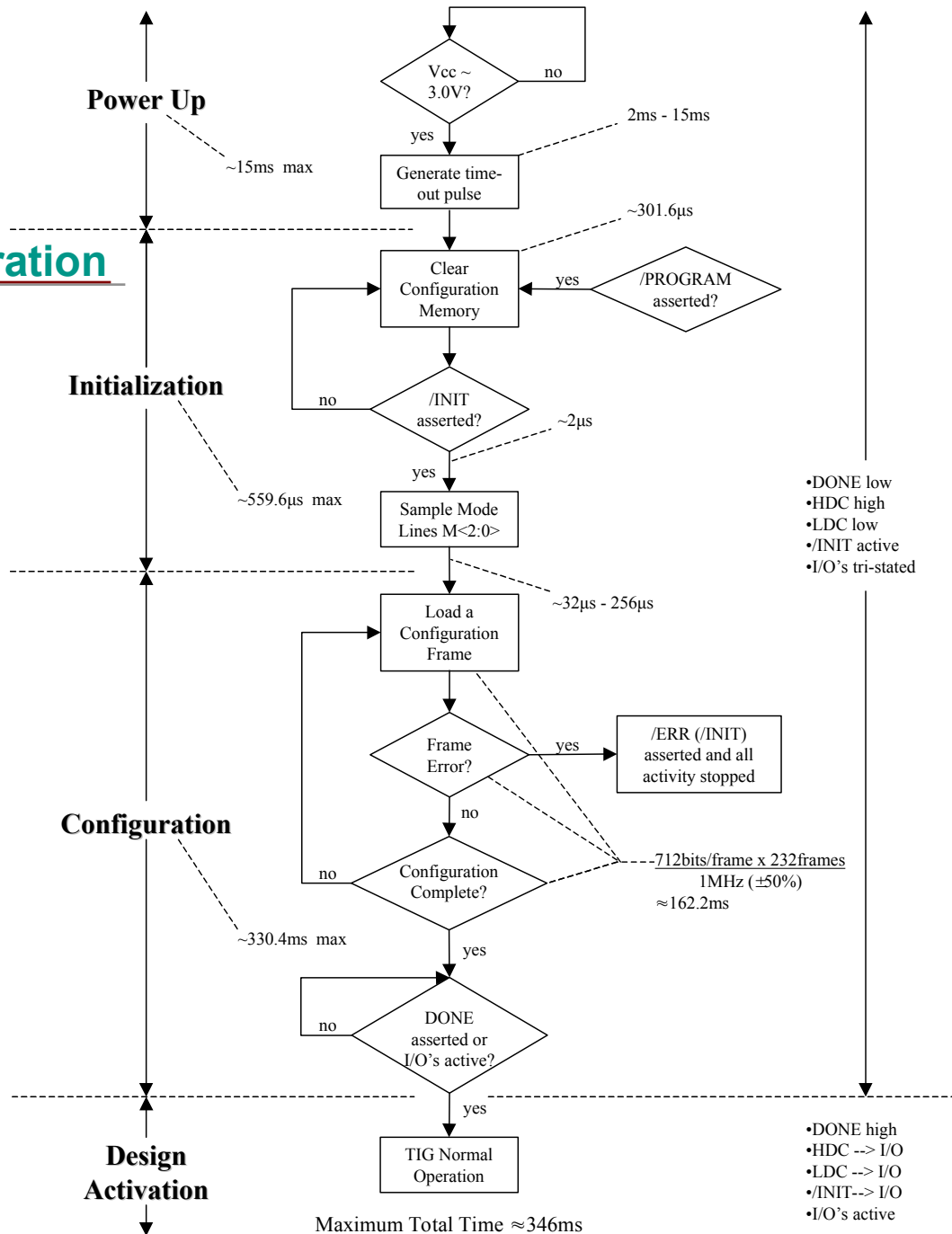
# System Integration



- The TIG Chip is an FPGA design in a 240-pin PQFP package
- Pin count break down:
  - 16  $V_{cc}$  (+5V)                      – 16 GND                      – 9 NC
  - 196 programmable I/O              – 3 fixed function
- The FPGA is programmed at power-up using data downloaded from a system Flash ROM.
- This allows the TIG to be upgraded via firmware updates; no need to open the box and replace parts
- A jumper selectable copy of the design resides in a fail-safe SRAM in case of Flash ROM corruption
- The TIG is powered by 5V; *not aux-5V*.
- Thus, the TIG is not alive when system power is OFF.



## TIG Self-Configuration Sequence



## Signs of Success

- the DONE pin is in a HI state
- the INIT/ERR pin is in a HI state
- byte at DPR location 00DA is set to AA (“TIG Alive”)
- power comes up and remains up
- at least one CPU begins SR0M tests

## Signs of Failure

- the DONE pin is in a LO state
- the INIT/ERR pin is in a LO state
- Remote Server Management console or the OCP reports a “TIG Failure”
- power comes up and immediately shuts down
- no CPU ever begins SR0M tests

## **Causes of TIG Configuration Failures**

---

- **5V power never comes up or comes up briefly**
  - If TIG configuration jumper is set to SROM mode, then the SROM may be blank, corrupt, or missing
  - Otherwise, the Flash ROM containing TIG design may be corrupt
- **5V is unstable (dips below 3.0V)**
  - power-power, power-ground, or power-chas short
  - bad regulators or power supplies
- **Flash ROM containing TIG design is corrupt**
  - try setting the TIG configuration jumper to SROM mode
- **TIG configuration SROM is corrupt, blank, or missing**
  - new, correctly programmed replacement SROM is *required*
  - try setting the TIG configuration jumper to Flash mode



- **Boundary scan logic**
  - TIG supports all mandatory boundary scan instructions
  - Holding INIT/ERR pin LO during power up will allow pre-configuration boundary scan testing of the FPGA
  - Dedicated TDI, TMS, and TCK pins allow boundary scan after TIG power-up and configuration.
- **Global output tristate pin**
  - Available only after TIG configuration
- **Test port**
  - 8-bit port available only after TIG configuration
  - Provides limited access to TIG internal registers and signals
- **TIG test card**
  - Available only in pre-FRS Clipper systems
  - SMT pads for the two test card connectors will still be accessible on the Clipper System Board post-FRS.

- ***TIG Specification (rev 3.52+)***
- ***Clipper Specification (rev 3.0+)***
- ***Clipper Serial SRAM Functional Specification***
- ***The Programmable Logic Data Book (by Xilinx®)***