



# Clipper System Board

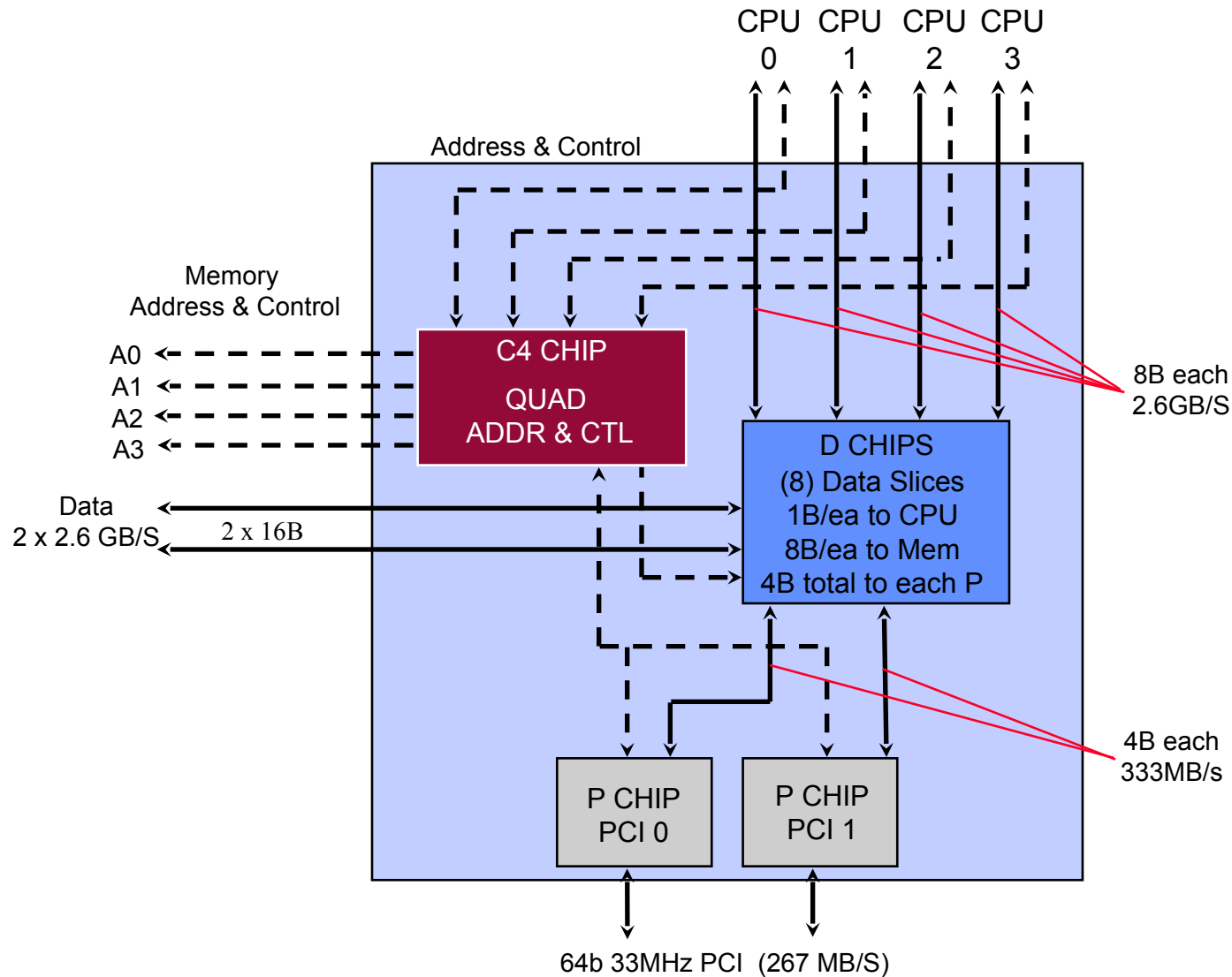
ETCH 50-25384-01

ASSY 54-25385-01

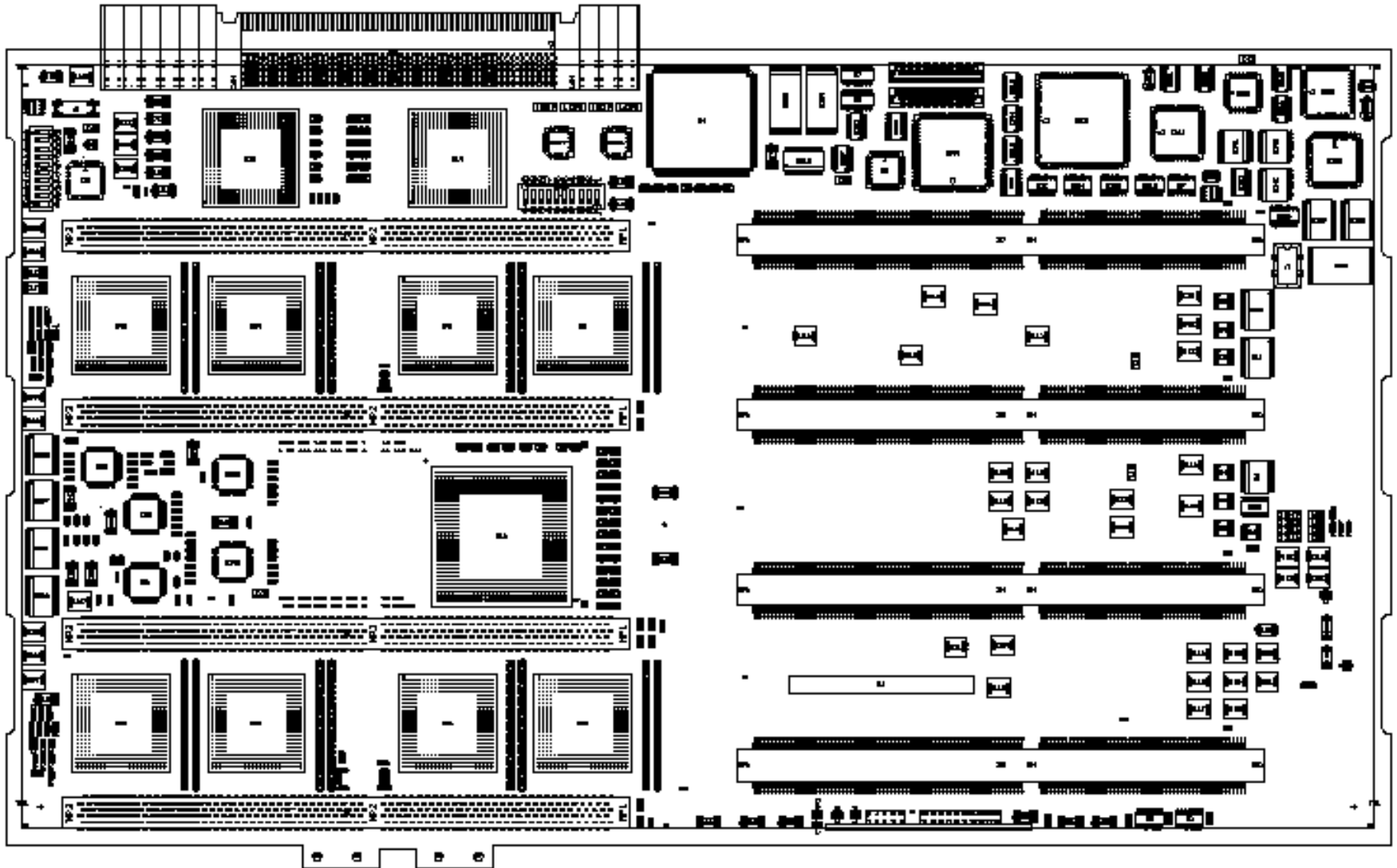
Dave Tatosian  
Alpha Volume Server Engineering

- **Supports 1 to 4 Alpha processor CPU modules**
  - EV6 CPUs are supported today
  - Support for future processors (eg: EV67)
- **Supports up to 32GB of synchronous DRAM memory**
  - 5.2 GB/Sec aggregate peak bandwidth to memory
- **Provides host bridges for 2 PCI buses**
  - Dual 64 bit, 33MHZ buses
  - 534 MB/Sec aggregate peak bandwidth
- **Central boot SRROM and control logic**
  - “TIG” chip, SRROM, and FLASH RAM, shared by all processors
- **Control logic for server management features**
  - System Power Control (“SPC”)
  - Remote Maintenance Console (“RMC”)
- **12 Layer FR4 module, .090” thick**

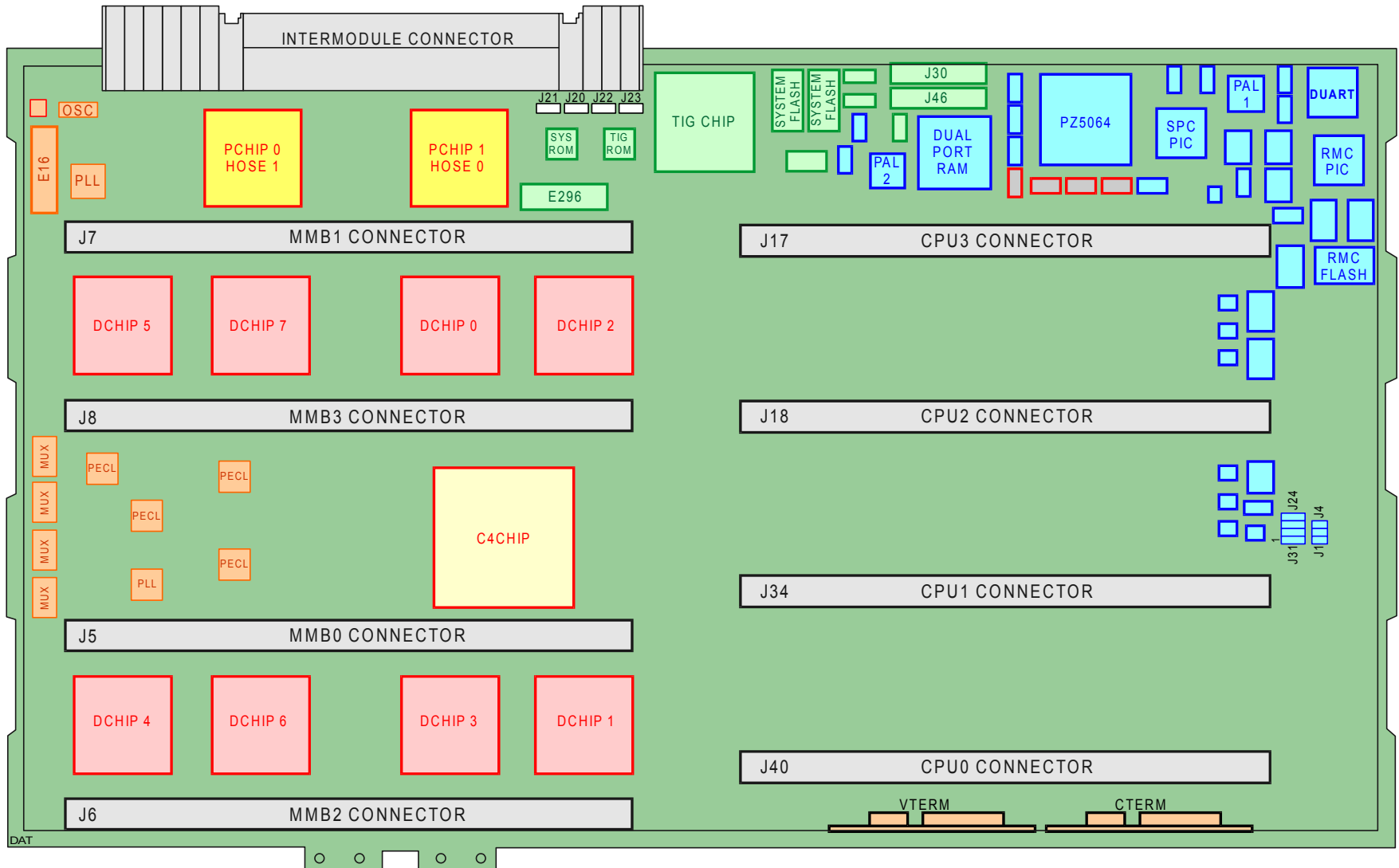
# System Board Core Logic



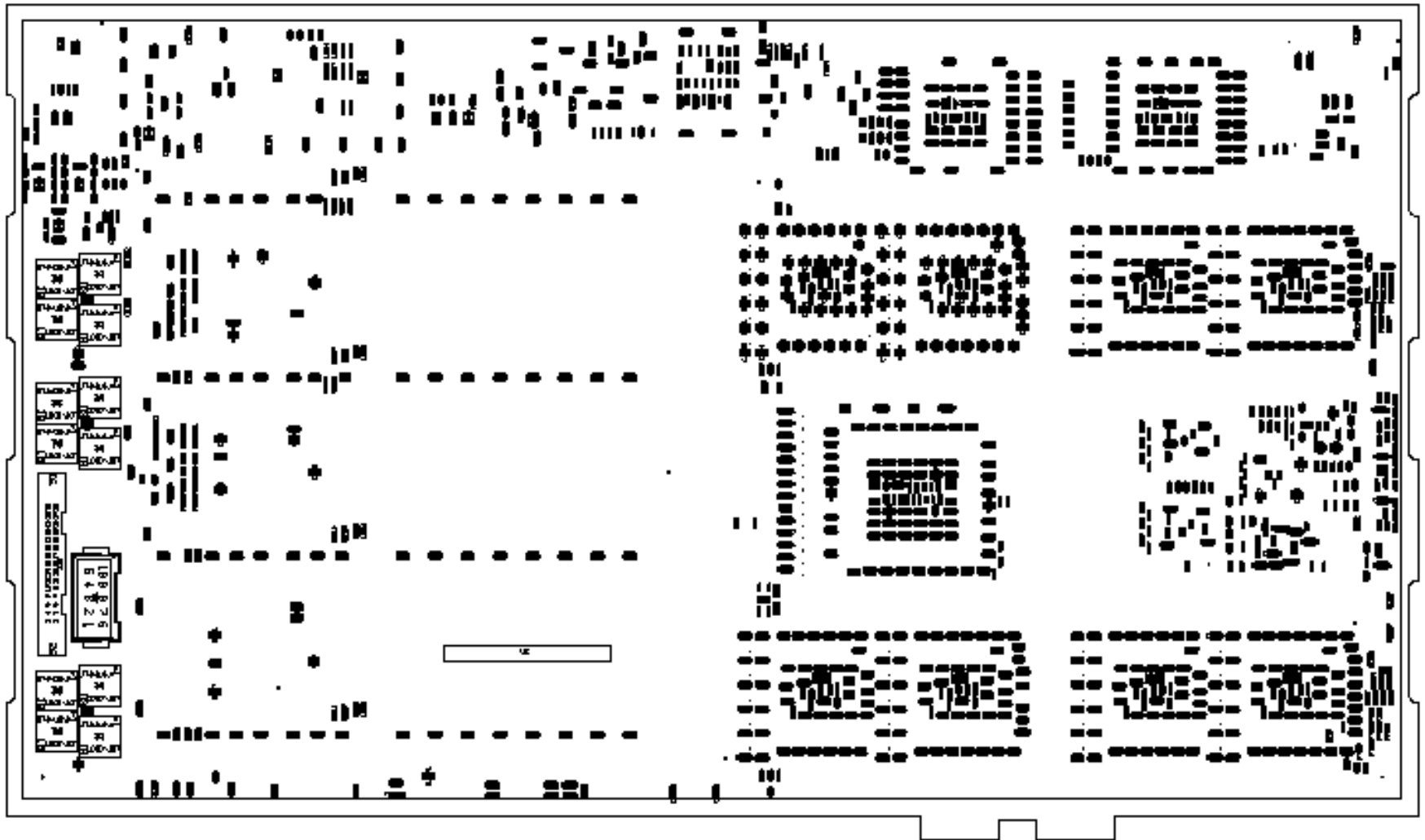
# CSB Assembly - Side 1 View



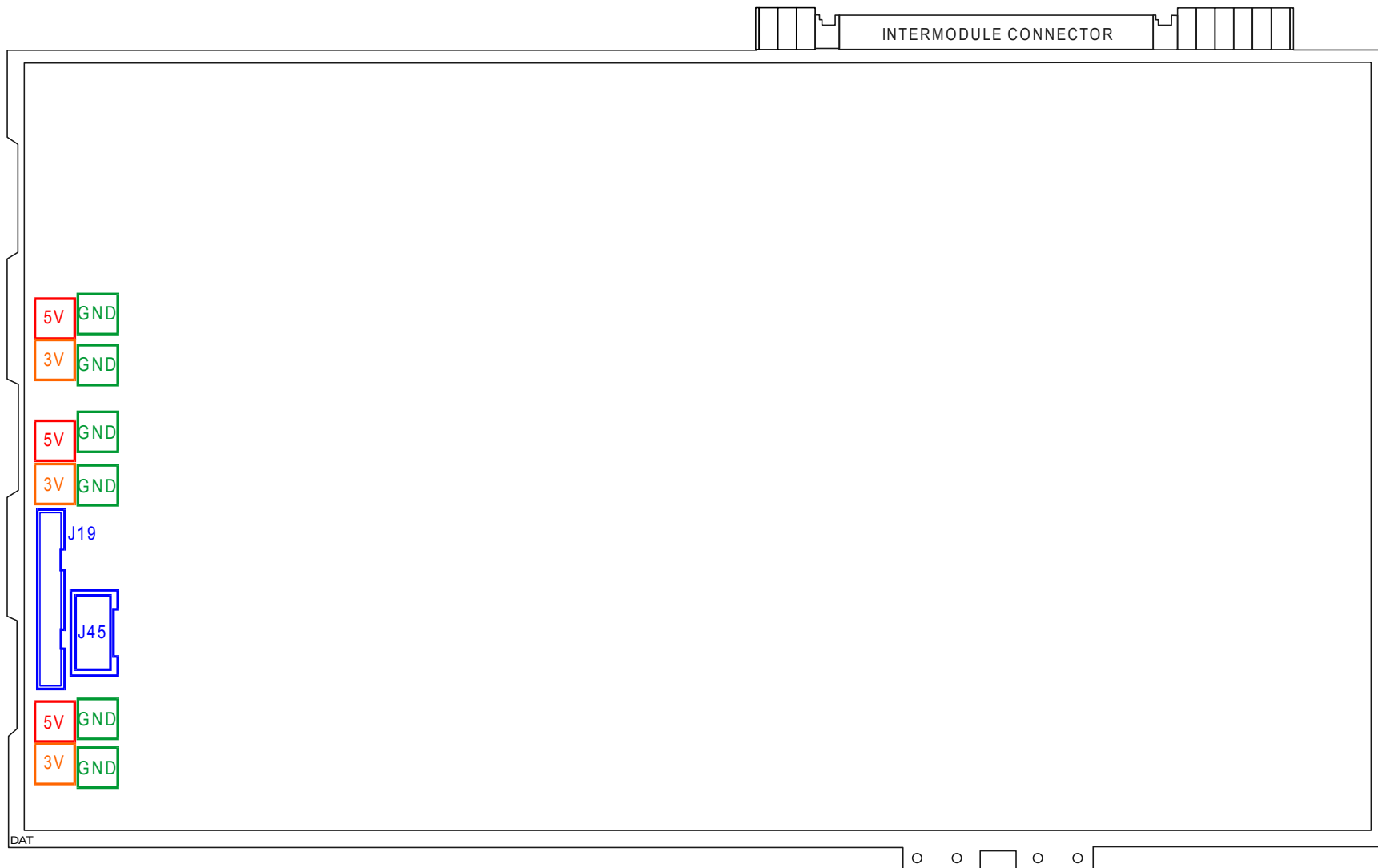
# CSB Logic Partitions



# CSB Assembly - Side 2 View



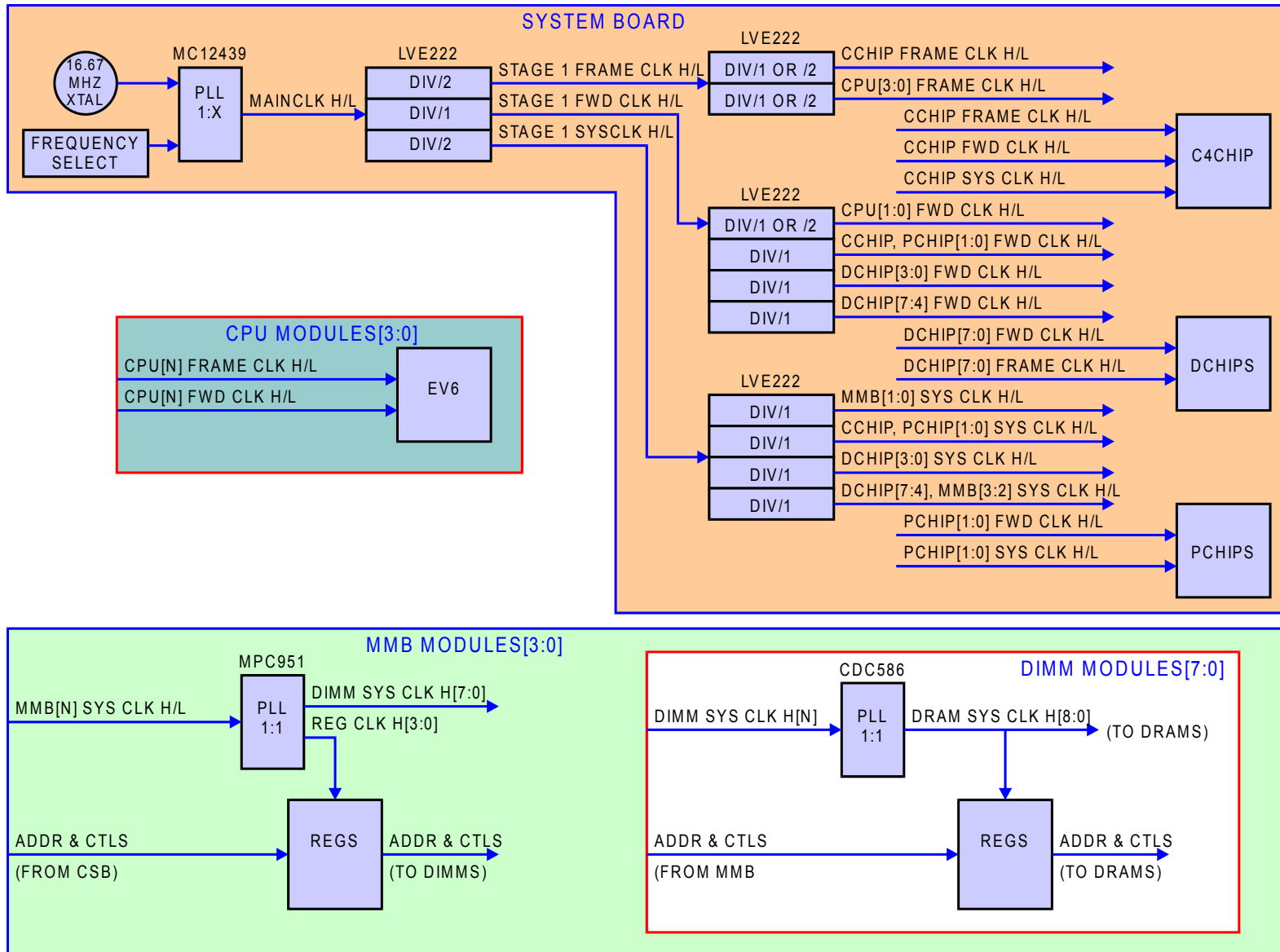
# CSB Power Cable Connectors



- **MAIN CLOCK (differential)**
  - Generated by PECL PLL
  - 16.67MHZ control frequency
  - 80 to 200MHZ in 16.67 MHZ steps
  - Used by core chipset and EV6 as FWDCLK
- **SYSCLK and FRAMECLK (differential)**
  - MAIN CLOCK divided by two
  - Used by core chipset, memory (MMB) and EV6
- **MMB provides PLL for fanout to DIMMs and registers (single ended)**
- **DIMM provides PLL for fanout to SDRAMs and registers (single ended)**
- **PChips divide FWDCLK 5 to provide 33 MHZ PCI bus clocks (single ended)**

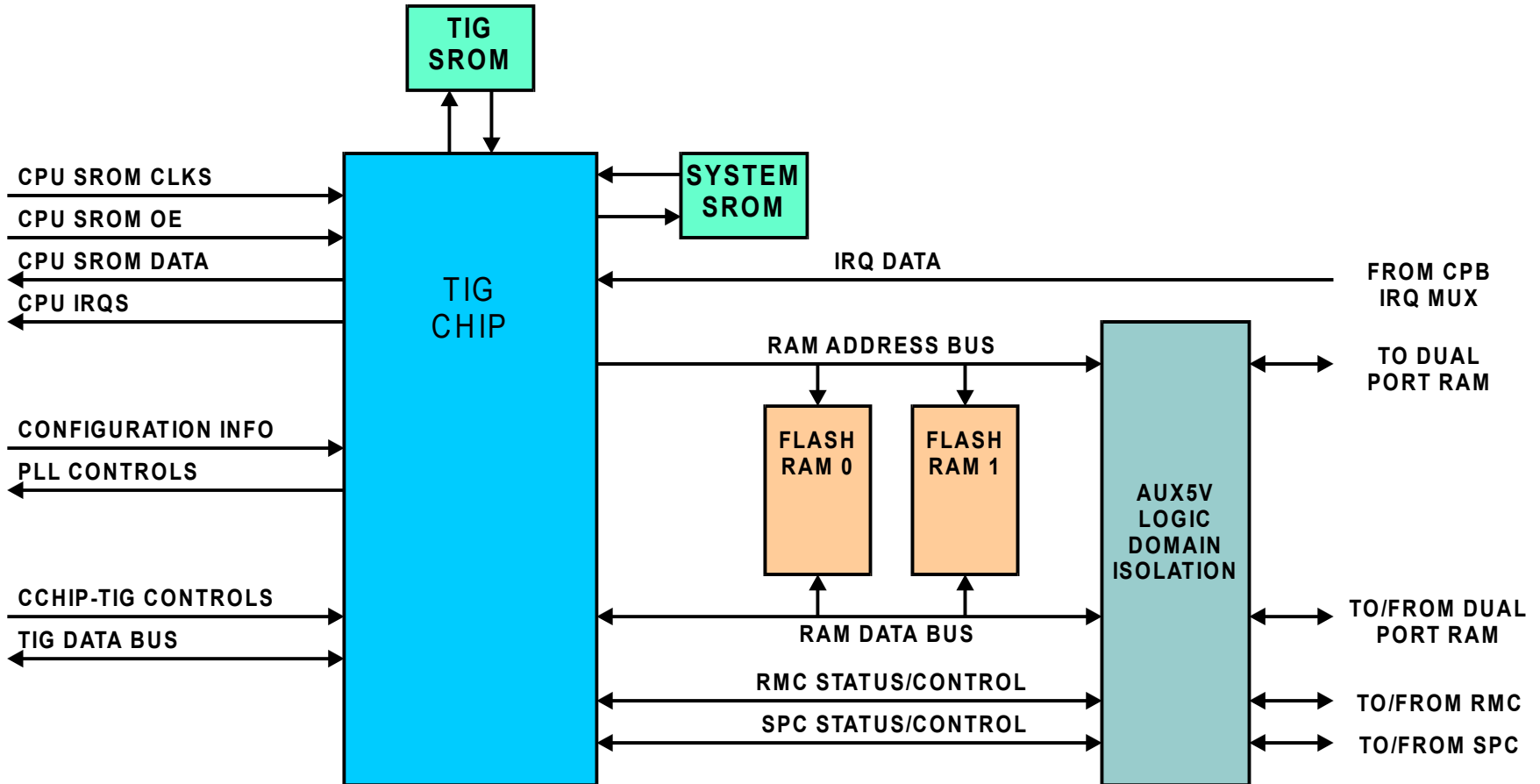


# System Clock Distribution



- **“Typhoon Interrupt and General Logic”**
- **Interface to OTP and FLASH SROM code stores**
- **Forwards interrupt data from CPB IRQ MUX to C-Chip**
- **IRQ generation to CPUs under C-Chip control**
- **General Purpose Registers**
  - Interprocessor Communication
  - Firmware information
  - System and environmental Status
  - “Switch and Jumper” interface
- **Controls CSB clock generation**
- **Provides firmware interfaces to RMC and SPC**
  - Coordinates CPU boot and speed settings with SPC
  - Allows message passing between firmware and RMC
    - System-side interface to Dual Ported SRAM

# TIG Bus Logic



- **System Power Control (“SPC”)**
  - Controls all power supplies and DC/DC converters
  - Initiates primary processor boot
  - Supports boot sequence of secondary processors
  - Manages low-level response to power component failures
- **Remote Maintenance Console (“RMC”)**
  - Remote interrogation and control of server complex
    - via terminal or modem connection
  - Manages cooling subsystem
  - Provides environmental monitoring (power, thermal status)
  - Generates status messages via OCP, terminal, modem and/or pager
- **Powered by AUX5V**
  - Always “alive” if line cord is installed

# Server Management Logic

