Serial ATA: An Evolutionary Transition

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Overview

The parallel ATA (AT Attachment) specification has defined the standard storage interface for PCs since the protocol was introduced in the 1980s. Parallel ATA has maintained its pre-eminence for three primary reasons: 1) low cost, 2) virtually universal operating system support, and 3) the ability of the specification to evolve to higher speed and performance while maintaining backward compatibility with older ATA devices. From its original speed of just 3 Mbytes/second, parallel ATA has moved up to a burst data transfer rate of 66 Mbytes/second. The latest generation of the interface, Ultra ATA-100, goes even further, with a burst data transfer rate of 100 Mbytes/second.

While ATA has enjoyed an illustrious track record, the specification is now showing its age. Parallel ATA imposes some serious design issues on today's developers, including a 5-volt signaling requirement, high pin count, and serious cabling headaches.

Intel Architecture Labs, in conjunction with the industry working group promoters and contributors, has developed the Serial ATA solution to overcome these design limitations while enabling the storage interface to scale with the growing media rate demands of PC platforms. Serial ATA is designed to be a software-transparent "drop-in" replacement for parallel ATA that maintains compatibility with existing operating systems and drivers, adding performance headroom for years to come. For these reasons, Serial ATA has attracted industry-wide support from PC OEMs, semiconductor manufacturers, and leading vendors of storage devices and software.

End of Parallel

All good things must come to an end, and parallel ATA is no exception. Here are the main reasons parallel ATA technology has run out of evolutionary headroom:

- *High pin count*. Parallel ATA requires 26 pins per channel. Multiplied by two channels, that's 56 pins per channel, plus power/ground.
- *High voltage*. Parallel ATA requires 5-volt transceivers, which impose integration problems with new silicon processes.
- *Cable problems*. The 80-conductor cable required to support parallel ATA is relatively expensive and unwieldy to route inside the PC chassis. Flat ribbon cable can interfere with air flow and cooling. To make matters worse, the ribbon header connector can be difficult to seat in the system board and the storage device during the assembly processes, and can lead to reliability and support issues.
- *Performance issues*. Evolving parallel ATA beyond 100 Mbytes/second could require the implementation of technical enhancements, including low voltage differential (LVD) signaling.

With approximately two years of lead time required to design and implement a new storage interface generation, this is a logical time for parallel ATA to evolve into a standard that can continue to support the price/performance requirements of desktop and mobile PC platforms. The software transparency and backward compatibility of Serial ATA specification makes it an even more compelling and timely solution for the industry.

Benefits of Serial ATA

The Serial ATA specification is designed to replace parallel ATA with a software-transparent interface for "inside the box" storage. It reduces voltage and pin count requirements and can be implemented with thin and easy to route cables.

- *Low voltage requirement*. Serial ATA requires only 500 millivolts (mV) peak-peak to support new silicon processes and higher integration.
- *Lower pin count*. Reducing the pin count helps reduce board real estate requirements and enables more reliable connections on the board and the storage device.
- *Higher integration*. Unlike parallel ATA, Serial ATA does not require 5-volt tolerant transceivers that can pose a hindrance to higher integration which utilize today's and future silicon processes.

Improved Air Flow with Serial ATA Cable

Ribbon Cable **Serial ATA Cable**

Figure 1

- *Better cabling*. As shown in Figure 1, Serial ATA replaces cumbersome ribbon cable with thin and flexible cable that can be up to one meter in length. Simpler cabling can reduce manufacturing cost, improve the reliability of cable connections, improve system cooling, and provide system designers more room inside the chassis.
- *Ideal for mobile*. The reduced power requirements make Serial ATA ideal for use in mobile PCs, enabling OEMs to use one standard interface across a broad line of cost-effective platforms.
- *Cost-effective*. At introduction, the cost of Serial ATA is expected to be competitive with today's parallel ATA implementations.
- *Software compatibility*. Serial ATA is a drop-in replacement for parallel ATA. There is no impact to the existing infrastructure of software and drivers.

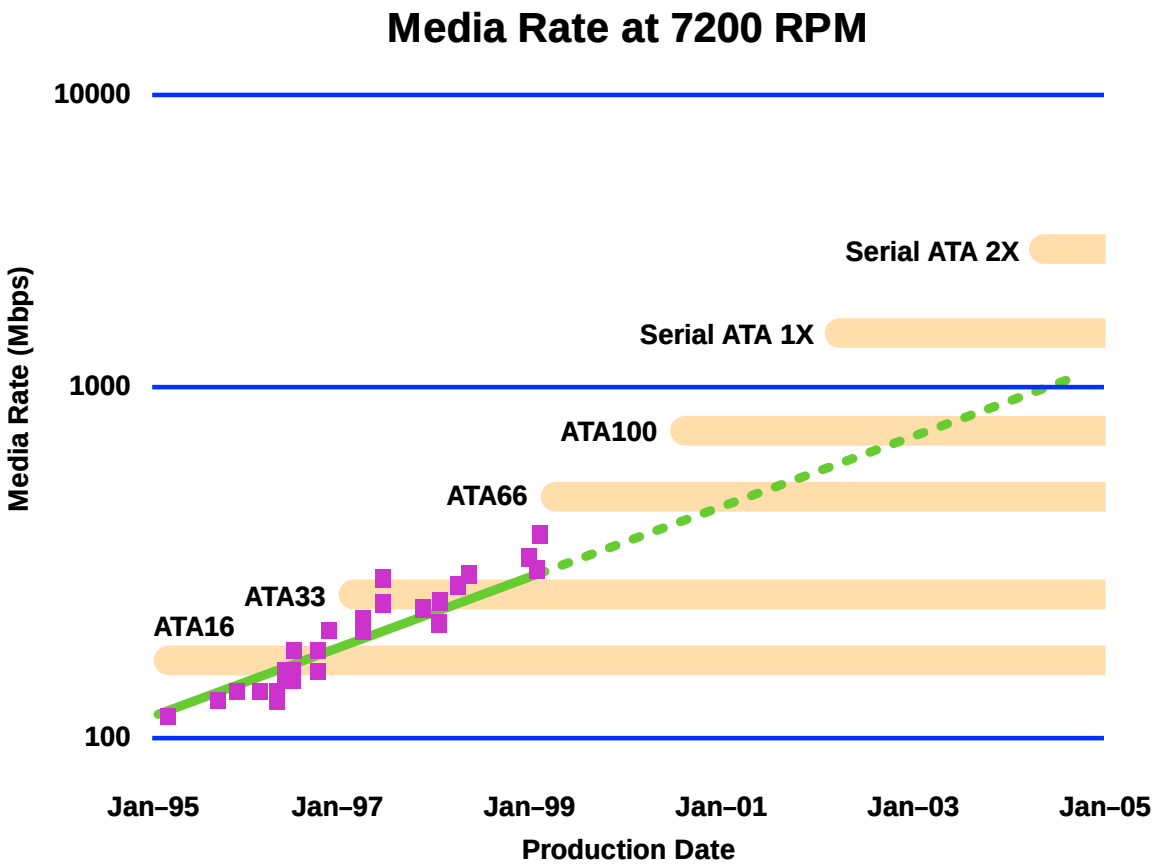

Figure 2

- *Strong roadmap*. As Figure 2 illustrates, the Serial ATA roadmap is currently projected to support scalability in successive generations of Serial ATA technology, beginning with a data rate of 150 Mbytes/second and evolving to data rates of 300 Mbytes/second and beyond.
- *Superset Features*. Serial ATA supports a superset of features including dynamic plug/unplug, addressing of drives larger than 137 Gbytes, first-party Direct Memory Access (DMA) and efficient command queuing. It's important to note that these features are not required for baseline functionality, and they will require additional software support.

When?

The 0.9 version of the Serial ATA specification is scheduled to be released at the Intel Developer Forum Conference, Fall 2000 (IDF). The goal is to have the 1.0 version of the specification completed by the end of this year. The introduction of first-generation Serial ATA devices capable of supporting 1.5-Gbit/second signaling is anticipated in mid-2001.

It is anticipated that transitional solutions will require discrete Serial ATA components in concert with chipsets that support Parallel ATA devices. Serial ATA chipsets are now under development by several third-party vendors. Attending the IDF Conference Fall 2000 may provide an opportunity to see the first Serial ATA chipsets from these suppliers.

As a transition strategy, developers may also use serial and parallel dongles to adapt parallel devices to a serial controller or adapt serial devices to a parallel controller.

Summary

The familiar parallel ATA interface has been the primary “inside the box” storage interface for more than 10 years. For a variety of reasons, including relatively high voltage requirements, cabling issues, and lack of performance headroom, a new solution is now required in order to keep pace with the growing media rate of desktop and mobile PCs.

In a development role similar to the one it took with PCI and USB technologies, Intel Architecture Labs is leading an industry working group that has developed a new interface specification designed as a drop-in replacement for the parallel ATA interface. Known as Serial ATA, this new serial interface is designed to overcome the limitations of parallel ATA while launching a roadmap that could drive 10 more years of storage interface performance evolution.

Thanks to its combination of software transparency, low cost, scalability, and design flexibility, Serial ATA has attracted widespread industry support through the Serial ATA Working Group. Membership in the working group provides developers with early access to the specification and influence over finalization and information, which can speed the transition to this innovative and cost-effective new storage interface technology.

More Info

More information about the Serial ATA specification and the benefits of membership in the Serial ATA Working Group is available on the Serial ATA Working Group Web site.

Plan to attend the Intel Developer Forum Conference Fall 2000 for the latest information on implementing the Serial ATA specification. Watch Intel’s Developer Web site for details.

Author Bio

In his role as marketing manager for the Intel Architecture Labs, Bill Colson oversees a wide range of technologies in the areas of platform architecture, voice/speech/media/data, and Internet services. During his 16-year career at Intel, Bill has been involved in the development of the Multibus I and Multibus II single board computers, and desktop and server technologies, including the first Intel® 386 PC baseboard. Bill holds a patent in the field of server management. He is a recipient of the Intel Achievement Award, and a former member of the IEEE and Next-Generation I/O Forum. A frequent contributor to *Intel Developer Update*, he has written articles for *EE Times* and *Electronic Design.* Bill holds a B.S. in computer systems engineering and electrical engineering from the Oregon Institute of Technology.

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