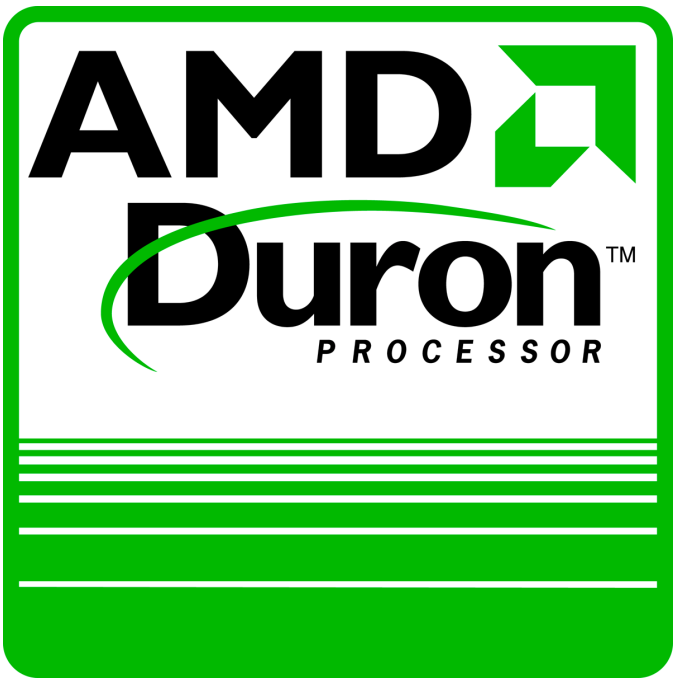
Preliminary Information

AMD Duron™

Processor Model 3
Data Sheet



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Revision History

Date	Rev	Description
October 2000	F	Revised VID[4:0] information in Table 3 on page 22 and "VID[4:0] Pins" on page 65
October 2000	E	Added information about the 800 MHz AMD Duron™ Processor Model 3 as follows: ■ Table 1, "Thermal Design Power," on page 19 ■ Table 6, "Operating Ranges," on page 23 ■ Table 8, "VCC_CORE Voltage and Current," on page 24 ■ Added AMD Athlon to the trademark list ■ Updated "Motherboard PGA Design Guide, order# 90009" with new document name of "Socket A Motherboard Design Guide, order# 24363" throughout book ■ Added SAI#[0] pin in location AJ29 to Figure 15, "AMD Duron™ Processor Model 3 Pin Diagram—Topside View" on page 44 ■ Added the AMD Pin (AH6) to Table 17, "Socket A Pin Cross-Reference by Pin Location," on page 53 and to the Pin Descriptions on page 60 ■ Revised all no connect (NC) pins on the pin grid array (PGA) as follows: ● Figure 15, "AMD Duron™ Processor Model 3 Pin Diagram—Topside View" on page 44 ● Table 16, "Pin Name Abbreviations," on page 45 ● Table 17, "Socket A Pin Cross-Reference by Pin Location," on page 53 ■ Revised "K7CLKOUT and K7CLKOUT# Pins" description on page 63 ■ Updated the ordering information on page 69
September 2000	D	Added information about the 750 MHz AMD Duron™ Processor Model 3 processor as follows: ■ Table 1, "Thermal Design Power," on page 19 ■ Table 6, "Operating Ranges," on page 23 ■ Table 8, "VCC_CORE Voltage and Current," on page 24

Date	Rev	Description
August 2000	C	■ Added Table 1, "Thermal Design Power," on page 19 ■ Revised VCC_CORE to 1.6 in Table 7, "Operating Ranges," on page 24 ■ Revised and reorganized the AC and DC characteristics for SYSCLK and SYSCLK#. See Table 11, "SYSCLK and SYSCLK# AC Characteristics," on page 27, and Table 10, "SYSCLK and SYSCLK# DC Characteristics," on page 26 ■ Added Table 15, "Miscellaneous Pins AC and DC Characteristics" on page 30 ■ Revised mechanical drawings in Chapter 8, pages 38 - 40 ■ Made corrections and updates to Chapter 9, "Pin Descriptions", in particular Table 19, "Socket A Pin Cross-Reference by Pin Location," on page 51 ■ Revised OPN from 4 digits to 3 (i.e. *from* 0550=0550 MHz *to* 550 MHz) in Chapter 10, "Ordering Information" on page 69
June 2000	B	Initial public release

1 Overview

The AMD Duron™ Processor Model 3 enables an optimized PC solution for value-conscious business and home users by providing the capability and flexibility to meet their computing needs for both today and tomorrow.

The AMD Duron™ Processor Model 3 is the latest offering from AMD designed for the value segment of the market. The innovative design was developed to accommodate new and more advanced applications, meeting the requirements of today's most demanding value-conscious buyers without compromising their budget.

Delivered in a PGA package, the AMD Duron Processor Model 3 is the new AMD workhorse processor for value desktop systems, delivering the highest integer, floating-point and 3D multimedia performance for applications running on x86 system platforms. The AMD Duron Processor Model 3 provides value-conscious customers with access to advanced technology that allows their system investment to last for years to come. The AMD Duron Processor Model 3 is designed as a solid platform for surfing the Internet, digital entertainment, and personal creativity. In addition, it is engineered to enable superior business productivity by delivering an optimized combination of computing performance and value.

The AMD Duron Processor Model 3 features the seventh-generation microarchitecture with an integrated L2 cache, which supports the growing processor and system bandwidth requirements of emerging software, graphics, I/O, and memory technologies. The AMD Duron Processor Model 3 high-speed execution core includes multiple x86 instruction decoders, a dual-ported 128-Kbyte split level-one (L1) cache, a 64-Kbyte on-chip L2 cache, three independent integer pipelines, three address calculation pipelines, and a superscalar, fully pipelined, out-of-order, three-way floating-point engine. The floating-point engine is capable of delivering superior performance on numerically complex applications.

The AMD Duron Processor Model 3 microarchitecture incorporates enhanced 3DNow!™ technology, a

high-performance cache architecture, and the 200-MHz 1.6-Gigabyte per second AMD system bus. The AMD system bus combines the latest technological advances, such as point-to-point topology, source-synchronous packet-based transfers, and low-voltage signaling, to provide the most powerful, scalable bus available for any x86 processor.

The AMD Duron Processor Model 3 is binary-compatible with existing x86 software and backwards compatible with applications optimized for MMX™ and 3DNow! instructions. Using a data format and single-instruction multiple-data (SIMD) operations based on the MMX instruction model, the AMD Duron Processor Model 3 can produce as many as four, 32-bit, single-precision floating-point results per clock cycle. The enhanced 3DNow! technology implemented in the AMD Duron Processor Model 3 includes new integer multimedia instructions and software-directed data movement instructions to deliver a superior performance to Celeron in multimedia and number-intensive applications.

1.1 AMD Duron™ Processor Model 3 Microarchitecture Summary

The following features summarize the AMD Duron Processor Model 3 microarchitecture:

- The industry's first nine-issue, superpipelined, superscalar x86 processor microarchitecture designed for high clock frequencies
- Multiple x86 instruction decoders
- Three out-of-order, superscalar, fully pipelined floating-point execution units, which execute all x87 (floating-point), MMX and 3DNow! instructions
- Three out-of-order, superscalar, pipelined integer units
- Three out-of-order, superscalar, pipelined address calculation units
- 72-entry instruction control unit
- Advanced dynamic branch prediction
- Enhanced 3DNow! technology with new instructions to enable improved integer math calculations for speech or video encoding and improved data movement for internet plug-ins and other streaming applications

- 200-MHz AMD system bus (scalable beyond 400 MHz) enabling leading-edge system bandwidth for data movement-intensive applications
- High-performance cache architecture featuring an integrated 128-Kbyte L1 cache and a 16-way, on-chip 64-Kbyte L2 cache

The AMD Duron Processor Model 3 delivers superior system performance in a cost-effective, industry-standard form factor. The AMD Duron Processor Model 3 is compatible with motherboards based on AMD's Socket A. Figure 1 shows a typical AMD Duron Processor Model 3 system block diagram.

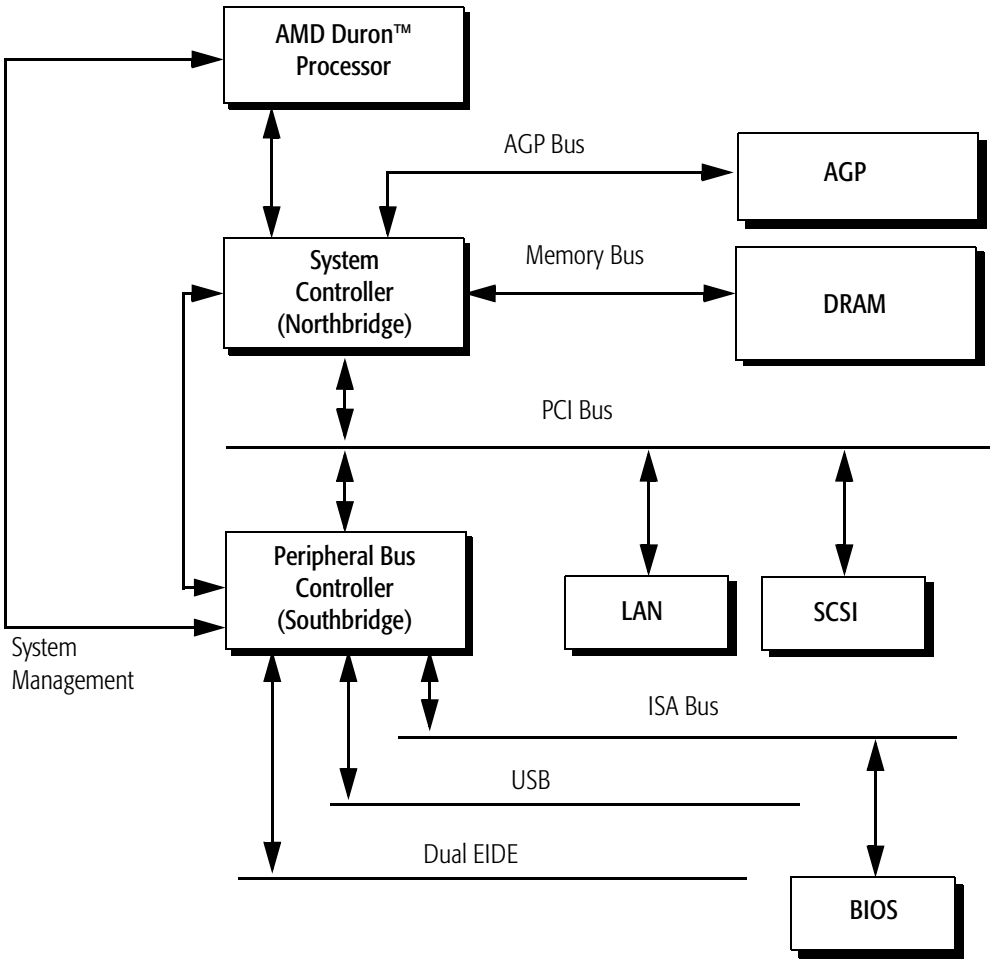


Figure 1. Typical AMD Duron™ Processor Model 3 System Block Diagram

2 Interface Signals

2.1 Overview

The AMD system bus architecture is designed to deliver superior data movement bandwidth for value x86 platforms. The system bus architecture consists of three high-speed channels (a unidirectional processor request channel, a unidirectional probe channel, and a 72-bit bidirectional data channel, including 8-bit error code correction [ECC] protection), source-synchronous clocking, and a packet-based protocol. In addition, the system bus supports several control, clock, and legacy signals. The interface signals use an impedance controlled push-pull low-voltage swing signaling technology contained within the Socket A mechanical connector, which is mechanically compatible with the industry-standard SC242 connector. For more information, see "AMD System Bus Signals" on page 6, Chapter 9, "Pin Descriptions" on page 43, and the *AMD System Bus Specification*, order# 21902.

2.2 Signaling Technology

The AMD system bus uses a low-voltage, swing signaling technology, which has been enhanced to provide larger noise margins, reduced ringing, and variable voltage levels. The signals are push-pull and impedance compensated. The signal inputs use differential receivers, which require a reference voltage (V_{REF}). The reference signal is used by the receivers to determine if a signal is asserted or deasserted by the source. Termination resistors are not needed because the driver is impedance matched to the motherboard and a high impedance reflection is used at the receiver to bring the signal past the input threshold.

For more information about pins and signals, see Chapter 9, "Pin Descriptions" on page 43.

2.3 Push-Pull (PP) Drivers

The Socket A AMD Duron™ Processor Model 3 supports Push-Pull (PP) drivers. The system logic configures the AMD Duron Processor Model 3 with the configuration parameter called SysPushPull (1=PP). The impedance of the PP drivers is set to match the impedance of the motherboard by two external resistors connected to the ZN and ZP pins. See "ZN, VCC_Z, ZP, and VSS_Z Pins" on page 66 for more information.

2.4 AMD System Bus Signals

The AMD system bus is a clock-forwarded, point-to-point interface with the following three point-to-point channels:

- A 13-bit unidirectional output address/command channel
- A 13-bit unidirectional input address/command channel
- 72-bit bidirectional data channel

For more information, see Chapter 6, "Electrical Data" on page 21 and the *AMD System Bus Specification*, order# 21902.

3 Logic Symbol Diagram

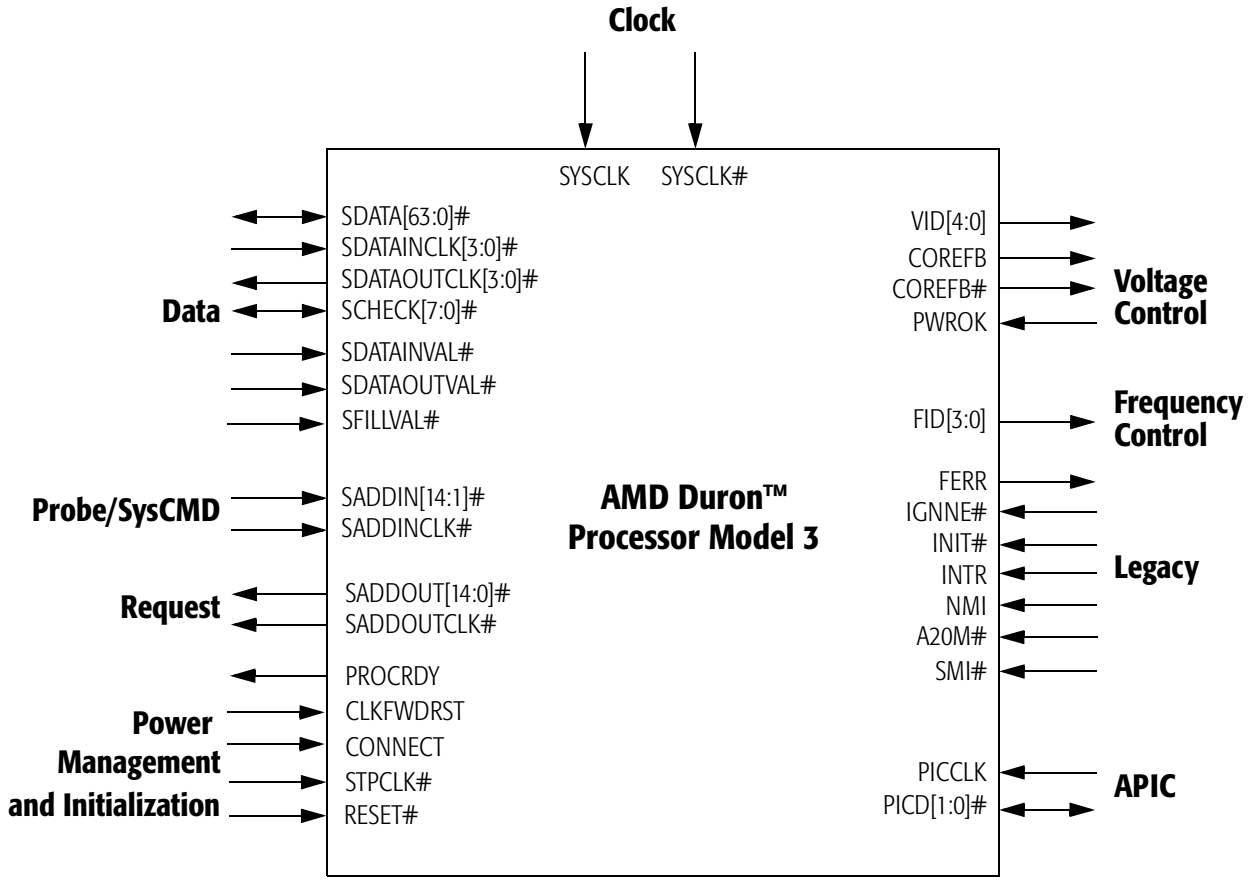
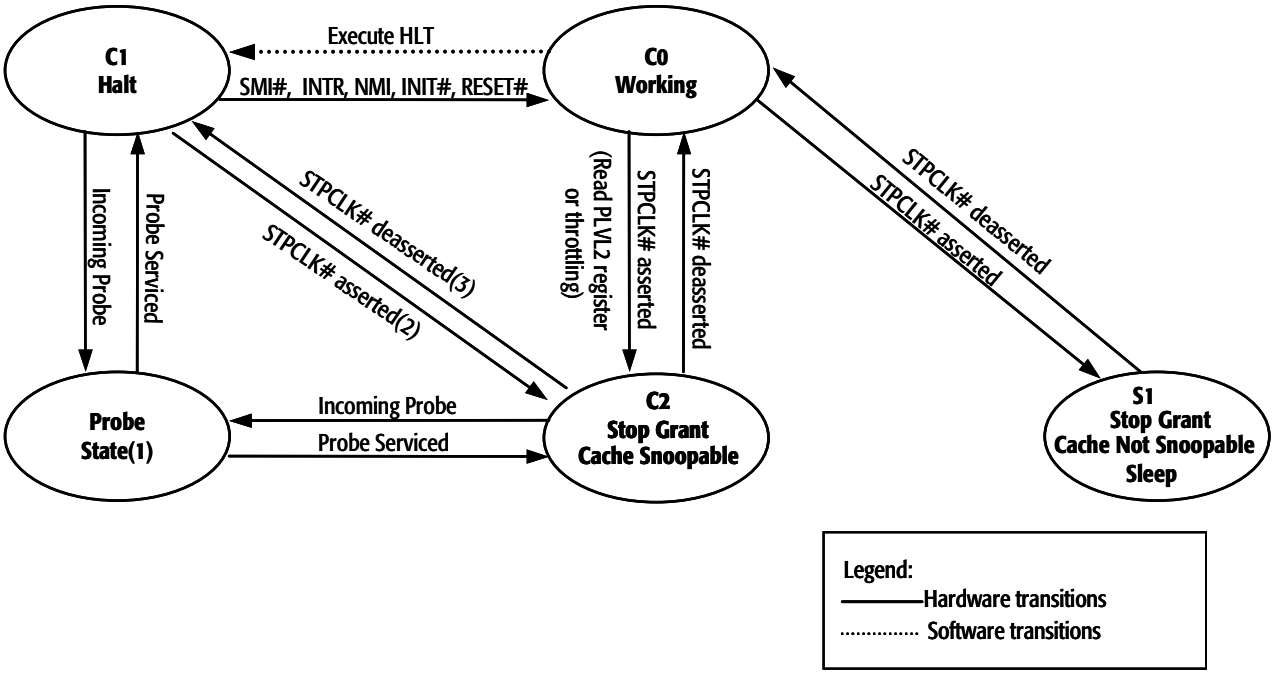


Figure 2. Logic Symbol Diagram

4 Power Management

4.1 Power Management States

The AMD Duron™ Processor Model 3 supports low-power Halt and Stop Grant states. These states are used by Advanced Configuration and Power Interface (ACPI) enabled operating systems for processor power management. Figure 3 shows the power management states of the AMD Duron Processor Model 3. The figure includes the ACPI "Cx" naming convention for these states.



Note: *The AMD System Bus is connected during:*
(1) The Probe state

(2) During transitions directly from the Halt state to the Stop Grant State, and

(3) Stop Grant state to the Halt state.

Figure 3. AMD Duron™ Processor Model 3 Power Management States

The following paragraphs describe each of the power management states.

Note: *In all power management states, the system must not disable the system clock (SYSCLK/SYSCLK#) to the processor.*

Working State

The Working state refers to the state in which the processor is executing instructions.

Halt State

When the AMD Duron Processor Model 3 executes the HLT instruction, the processor issues a Halt special cycle to the system bus. The phase-lock loop (PLL) continues to run, enabling the processor to monitor bus activity and provide a quick resume from the Halt state. The processor enters a lower power state if the system logic (Northbridge) disconnects the AMD System Bus in response to the Halt special cycle.

The Halt state is exited when the processor samples INIT#, INTR, NMI, RESET#, or SMI# asserted.

Stop Grant States

The AMD Duron Processor Model 3 enters the Stop Grant state upon recognition of assertion of STPCLK# input. There are two mechanisms for asserting STPCLK# – hardware and software. The Southbridge can force STPCLK# assertion for throttling to protect the processor from exceeding its maximum case temperature. This is accomplished by asserting the THERM# input to the Southbridge. Throttling asserts STPCLK# for a percentage of a predefined throttling period: STPCLK# is repetitively asserted and deasserted until the THERM# pin is deasserted.

Software can force the processor into the Stop Grant state by accessing ACPI-defined registers typically located in the Southbridge. Software places the processor in C2 by reading the PLVL_2 register in the Southbridge. In C2, probes are allowed, as shown in Figure 3 on page 9.

If an ACPI Thermal Zone is defined for the processor, the OS can initiate throttling with STPCLK# using the ACPI defined P_CNT register in the Southbridge. The processor enters the Probe state to service cache snoops initiated by the Northbridge during Stop Grant for C2 or throttling.

The Stop Grant state is also entered for the S1 system sleep state based on a write to the SLP_TYP field in the ACPI-defined

power management 1 control register. During the S1 sleep state, system software ensures no bus master or probe activity occurs.

After recognizing the assertion of STPCLK#, the AMD Duron Processor Model 3 completes all pending and in-progress bus cycles and acknowledges the STPCLK# assertion by issuing a Stop Grant special bus cycle to the AMD system bus. After the Northbridge disconnects the AMD system bus in response to the Stop Grant special bus cycle, the processor enters a low-power state dictated by the CLK_Ctl register. During the Stop Grant states, the processor latches INIT#, INTR (if interrupts are enabled), NMI, and SMI#, if they are asserted.

The Stop Grant state is exited upon the deassertion of STPCLK# or the assertion of RESET#. When STPCLK# is deasserted, the processor will initiate a connection of the AMD System Bus if it is disconnected. After the processor enters the Working state, any pending interrupts are recognized and serviced and the processor resumes execution at the instruction boundary where STPCLK# was initially recognized.

If RESET# is sampled asserted during the Stop Grant state, the processor returns to the Working state and the reset process begins.

Probe State

The Probe state is entered when the Northbridge initiates an AMD system bus connect as required to probe the processor. If the processor has been disconnected from the system bus, the Northbridge must initiate a system bus connection prior to probing the processor to snoop the processor's caches for example. When in the Probe state, the processor responds to a probe cycle in the same manner as when it is in the Working state.

When the probe has been serviced, the processor returns to the same state as when it entered the Probe state (Halt or Stop Grant state). Once in the Halt or Stop Grant state, a low-power state is only achieved if the Northbridge initiates a disconnection from the system bus.

4.2 Connect and Disconnect Protocol

Significant power savings of the AMD Duron Processor Model 3 only occurs if the processor is disconnected from the system bus by the Northbridge while in the Halt or Stop Grant state. The Northbridge can optionally initiate a bus disconnect upon the receipt of a Halt or Stop Grant special cycle. The option of disconnecting is controlled by an enable bit in the Northbridge. If the Northbridge requires the processor to service a probe after the system bus has been disconnected, it must first initiate a system bus connect.

Connect Protocol

In addition to the legacy STPCLK# signal and the Halt and Stop Grant special cycles, the AMD system bus connect protocol includes the CONNECT, PROCRDY, and CLKFWDRST signals and a *Connect* special cycle.

AMD system bus disconnects are initiated by the Northbridge in response to the receipt of a Halt or Stop Grant special cycle. Reconnect is initiated by the processor in response to an interrupt for Halt, STPCLK# deassertion, or by the Northbridge to service a probe.

The Northbridge contains BIOS programmable registers to enable the system bus disconnect in response to Halt and Stop Grant special cycles. When the Northbridge receives the Halt or Stop Grant special cycle from the processor and, if there are no outstanding probes or data movements, the Northbridge deasserts CONNECT a minimum of eight SYSCLK periods after the last command sent to the processor. The processor detects the deassertion of CONNECT on a rising edge of SYSCLK, and deasserts PROCRDY to the Northbridge. In return, the Northbridge asserts CLKFWDRST in anticipation of reestablishing a connection at some later point.

Note: *The Northbridge must disconnect the processor from the AMD system bus before issuing the Stop Grant special cycle to the PCI bus, or passing the Stop Grant special cycle to the Southbridge for systems which connect to the Southbridge with LDT.*

This note applies to current chipset implementation: alternate chipset implementations that do not require this are possible.

Note: *In response to Halt special cycles, the Northbridge passes the Halt special cycle to the PCI bus or Southbridge immediately.*

The processor can receive an interrupt after it sends a Halt special cycle, or STPCLK# deassertion after it sends a Stop Grant special cycle to the Northbridge but before the disconnect actually occurs. In this case, the processor sends the Connect special cycle to the Northbridge, rather than continuing with the disconnect sequence. In response to the Connect special cycle, the Northbridge cancels the disconnect request.

The system is required to assert the CONNECT signal before returning the C-bit for the connect special cycle (assuming CONNECT has been deasserted). For more information, see the *AMD Athlon™ System Bus Specification*, order# 21902 for the definition of the C-bit and the Connect special cycle.

Figure 4 shows the sequence of events from a Northbridge perspective, which leads to disconnecting the processor from the AMD system bus and placing the processor in the Stop Grant state.

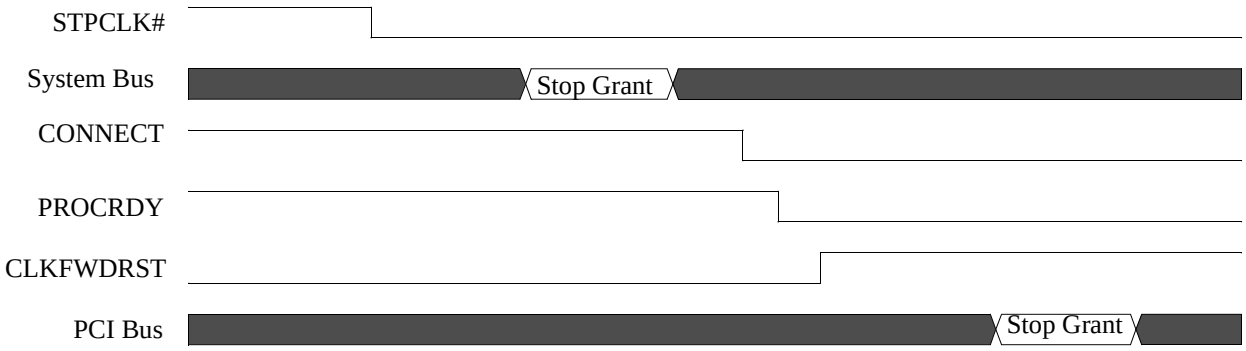


Figure 4. Example System Bus Disconnect Sequence

The following sequence of events describes how the processor is placed in the Stop Grant state when bus disconnect is enabled within the Northbridge:

1. The Southbridge asserts STPCLK# to place the processor in the Stop Grant state.
2. When the processor recognizes STPCLK# asserted and enters the Stop Grant State, the Southbridge issues a Stop Grant special bus cycle on the AMD system bus.

3. When the special cycle is received by the Northbridge and no probe traffic is pending, the Northbridge deasserts CONNECT, initiating a bus disconnect to the processor.
4. The processor responds to the Northbridge by deasserting PROCRDY, acknowledging the bus disconnect request.
5. The Northbridge asserts CLKFWDRST to complete the bus disconnect sequence.
6. After the processor is disconnected from the bus, the Northbridge passes the Stop Grant special cycle to the Southbridge via the PCI bus, notifying it that the processor is in the Stop Grant state.

Figure 5 shows the signal sequence of events that take the processor out of the Stop Grant state, reconnect the processor to the AMD system bus, and put the processor into the Working state.

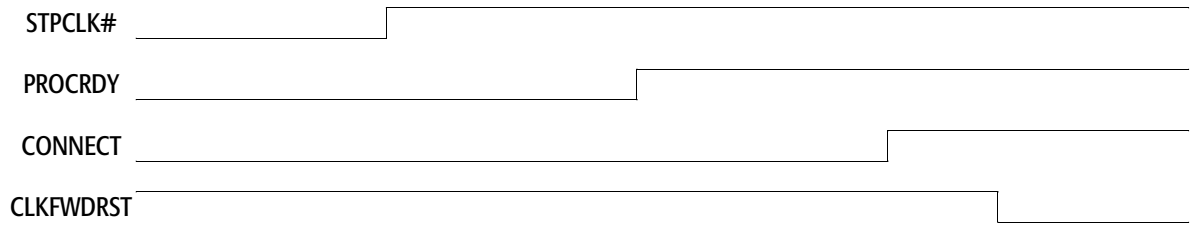


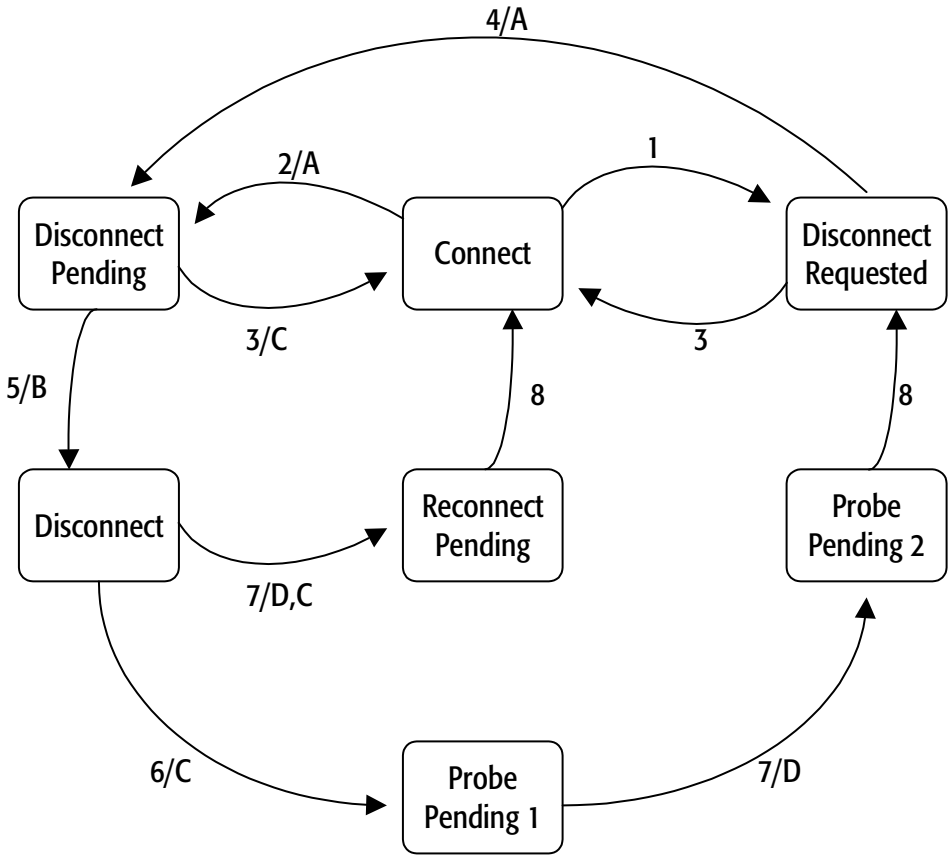
Figure 5. Exiting Stop Grant State/Bus Reconnect Sequence

The following sequence of events removes the processor from the Stop Grant state and reconnects it to the AMD system bus:

1. The Southbridge deasserts STPCLK# in response to a resume event.
2. When the processor recognizes STPCLK# deassertion, it asserts PROCRDY, notifying the Northbridge to reconnect to the bus.
3. The Northbridge asserts CONNECT.
4. The Northbridge finally deasserts CLKFWDRST, which synchronizes the forwarded clocks between the processor and the Northbridge.

Connect State Diagram

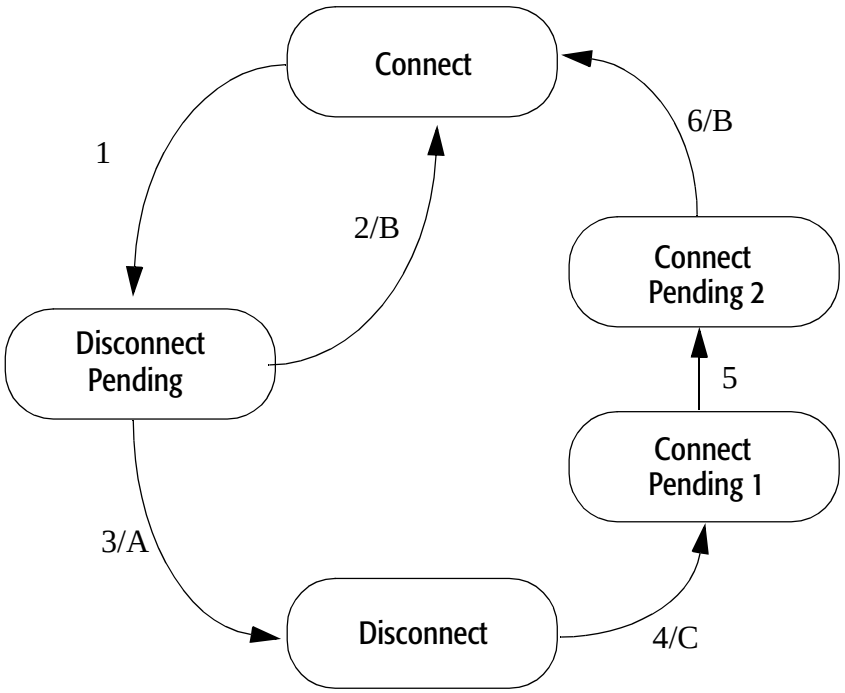
Figure 6 and Figure 7 describe the Northbridge and processor connect state diagrams, respectively.



	Condition
1	A disconnect is requested and probes are still pending
2	A disconnect is requested and no probes are pending
3	A CONNECT special cycle from the processor
4	No probes are pending
5	PROCRDY is deasserted
6	A probe needs service
7	PROCRDY is asserted
8	3 SYSCLK periods after CLKFWDRST is deasserted. *Although reconnected to the system interface, the Northbridge must not issue any non-NOP SysDC commands for a minimum of four SYSCLK periods after deasserting CLKFWDRST.*

	Action
A	Deassert CONNECT 8 SYSCLK periods after last SysDC sent
B	Assert CLKFWDRST
C	Assert CONNECT
D	Deassert CLKFWDRST

Figure 6. Northbridge Connect State Diagram



	Condition
1	CONNECT is deasserted by the Northbridge (for a previously sent Halt or Stop Grant special cycle).
2	Processor receives a wake-up event and must cancel the disconnect request.
3	Deassert PROCRDY and slow down internal clocks.
4	Processor wake-up event or CONNECT asserted by Northbridge.
5	CLKFWDRST is deasserted by the Northbridge.
6	Forward clocks start 3 SYSCLK periods after CLKFWDRST is deasserted.

	Action
A	CLKFWDRST is asserted by the Northbridge.
B	Issue a CONNECT special cycle.*
C	Return internal clocks to full speed and assert PROCRDY

** The Connect special cycle is only issued after a processor wake-up event (interrupt or STPCLK# deassertion) occurs. If the AMD system bus is connected so the Northbridge can probe the processor a Connect special cycle is not issued at that time (it is only issued after a subsequent processor wake-up event).*

Figure 7. Processor Connect State Diagram

4.3 Clock Control

The processor implements a Clock Control (CLK_Ctl) MSR (address C001_001Bh) that determines the internal clock divisor when the AMD system bus is disconnected.

Refer to the *AMD Athlon™ Processor BIOS Developers Guide*, order# 21656, for more details on the CLK_Ctl register.

5 Thermal Design

For information about thermal design, including layout and airflow considerations, see the *AMD Thermal, Mechanical, and Chassis Cooling Design Guide*, order# 23794 and the cooling guidelines on www.amd.com.

Table 1 shows the thermal design power. The thermal design power represents the maximum sustained power dissipated while executing publicly available software or instruction sequences under normal system operation at nominal VCC_CORE. Thermal solutions must monitor the processor temperature to prevent the processor from exceeding its maximum die temperature.

The maximum die temperature is specified through characterization at 90°C.

Table 1. Thermal Design Power

Frequency (MHz)	Voltage	Maximum Thermal Power	Typical Thermal Power
600	1.6 V	27.4 W	24.5 W
650		29.4 W	26.4 W
700		31.4 W	28.2 W
750		33.4 W	30.0 W
800		35.4 W	31.8 W

6 Electrical Data

6.1 Conventions

The conventions used in this chapter are as follows:

- Current specified as being sourced by the processor is *negative*.
- Current specified as being sunk by the processor is *positive*.

6.2 AMD Duron™ Processor Model 3 Interface Signal Groupings

The electrical data in this chapter is presented separately for each signal group. Table 2 defines each group and the signals contained in each group.

Table 2. AMD Duron™ Processor Model 3 Interface Signal Groupings

Signal Group	Signals	Notes
Power	VID[4:0], VCC_CORE, VCCA, COREFB, COREFB#	See "Voltage Identification (VID[4:0])" on page 22, "VID[4:0] Pins" on page 65, and "VCCA AC and DC Characteristics" on page 23.
Frequency	FID[3:0]	See "Frequency Identification (FID[3:0])" on page 22 and "FID[3:0] Pins" on page 62.
System Clocks	SYSCLK, SYSCLK# (Tied to CLKIN/CLKIN# and RSTCLK/RSTCLK#), PLLBYPASSCLK#, PLLBYPASSCLK	See "SYSCLK and SYSCLK# DC Characteristics" on page 25.
System Bus	SADDIN[14:2]#, SADDOUT[14:2]#, SADDINCLK#, SADDOUTCLK#, SFILLVAL#, SDATAINVAL#, SDATAOUTVAL#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAOUTCLK[3:0]#, SCHECK[7:0]#, CLKFWDRST, PROCRDY, CONNECT	See "AMD System Bus AC and DC Characteristics" on page 27.
Southbridge	RESET#, INTR, NMI, SMI#, INIT#, A20M#, FERR, IGNNE#, STPCLK#, FLUSH#	See "General AC and DC Characteristics" on page 29.
JTAG	TMS, TCK, TRST#, TDI, TDO	See "General AC and DC Characteristics" on page 29.
APIC	PICD[1:0]#, PICCLK	See "APIC Pins AC and DC Characteristics" on page 30.
Test	PLLTEST#, PLLMON1, PLLMON2, SCANCLK1, SCANCLK2, SCANSHIFTEN, SCANINTEVAL, ANALOG	See "General AC and DC Characteristics" on page 29.
Miscellaneous	DBREQ#, DBRDY, PWROK, PLLBYPASS#	See "General AC and DC Characteristics" on page 29.

6.3 Voltage Identification (VID[4:0])

Table 3 shows the VID[4:0] DC characteristics. For more information, see "VID[4:0] Pins" on page 65.

Table 3. VID[4:0] DC Characteristics

Parameter	Description	Min	Max
I_{OL}	Output Current Low		TBD
V_{OH}	Output High Voltage		

6.4 Frequency Identification (FID[3:0])

Table 4 shows the FID[3:0] DC characteristics. For more information, see "FID[3:0] Pins" on page 62.

Table 4. FID[3:0] DC Characteristics

Parameter	Description	Min	Max
I_{OL}	Output Current Low		TBD
V_{OH}	Output High Voltage		2.5 V*

Note:
* *The FID pins must not be pulled above this voltage by an external pullup resistor.*

6.5 VCCA AC and DC Characteristics

Table 5 shows the AC and DC characteristics for VCCA. For more information, see "VCCA Pin" on page 65.

Table 5. VCCA AC and DC Characteristics

Symbol	Parameter	Min	Max	Units
V_{VCCA}	VCCA Pin Voltage (DC)	2.25	2.75	V
I_{VCCA}	VCCA Pin Current	0	50	mA/GHz*
$V_{VCCA-NOISE}$	VCCA Pin Voltage (AC)	–100	+100	mV

Note:
* *Measured at 2.5 V*

6.6 Decoupling

See the *Socket A Motherboard Design Guide*, order# 24363, or contact your local AMD office for information about the decoupling required on the motherboard for use with the AMD Duron™ Processor Model 3.

6.7 Operating Ranges

The AMD Duron Processor Model 3 is designed to provide functional operation if the voltage and temperature parameters are within the limits defined in Table 6.

Table 6. Operating Ranges

Parameter	Description		Min	Nominal	Max	Notes
VCC_CORE	Processor core supply	600-800 MHz	1.5 V	1.6 V	1.7 V	1
VCC_CORE_{SLEEP}	Processor core supply in Sleep state		1.2 V	1.3 V	1.4 V	2
T_{DIE}	Temperature of processor die				90º C	

Notes:
1. *For normal operating conditions (nominal VCC_CORE is 1.6 V)*
2. *Sleep Voltage can be used for the S1 sleep state.*
   For more information see the Processor BIOS Developer's Guide, order# 21656.

6.8 Absolute Ratings

The AMD Duron Processor Model 3 should not be subjected to conditions exceeding the absolute ratings listed in Table 7, as such conditions may adversely affect long-term reliability or result in functional damage.

Table 7. Absolute Ratings

Parameter	Description	Min	Max
VCC_CORE	AMD Duron™ Processor Model 3 core supply	–0.5 V	VCC_CORE Max + 0.5 V
VCCA	AMD Duron Processor Model 3 PLL Supply	–0.5 V	VCCA Max + 0.5 V
V_{PIN}	Voltage on any signal pin	–0.5 V	VCC_CORE Max + 0.5 V
$T_{STORAGE}$	Storage temperature of processor	–40° C	100° C

6.9 VCC_CORE Voltage and Current

Table 8 shows the power and current of the processor during normal and reduced power states.

Table 8. VCC_CORE Voltage and Current

Frequency (MHz)	Nominal Voltage	Maximum Voltage	Stop Grant (Maximum)[1]	Maximum I_{CC} (Power Supply Current)[2]	Die Temperature
600	1.6 V	1.7 V	5 W	17.1 A	90°C
650				18.4 A	
700				19.6 A	
750				20.9 A	
800				22.1 A	

Notes:

1 *Measured at 1.3 V for Sleep state operating conditions. The BIOS must program the CLK_Ctrl MSR to 2967_9223h for the AMD Duron Processor Model 3.*

2. *Measured at Nominal Voltage*

Table 9 shows the DC characteristics of the SYSCLK and SYSCLK# differential clocks. The SYSCLK signal represents CLKIN and RSTCLK tied together while the SYSCLK# signal represents CLKIN# and RSTCLK# tied together. Figure 8 shows this condition.

Table 9. SYSCLK and SYSCLK# DC Characteristics

Symbol	Description	Min	Max	Units
$V_{Threshold-DC}$	Crossing before transition is detected (DC)	400		mV
$V_{Threshold-AC}$	Crossing before transition is detected (AC)	450		mV
I_{LEAK_P}	Leakage current through P-channel pullup to VCC_CORE	−1		mA
I_{LEAK_N}	Leakage current through N-channel pulldown to VSS (Ground)		1	mA
V_{CROSS}	Differential signal crossover		VCC_CORE/2 +/− 100	mV
C_{PIN}	Capacitance	4	12	pF

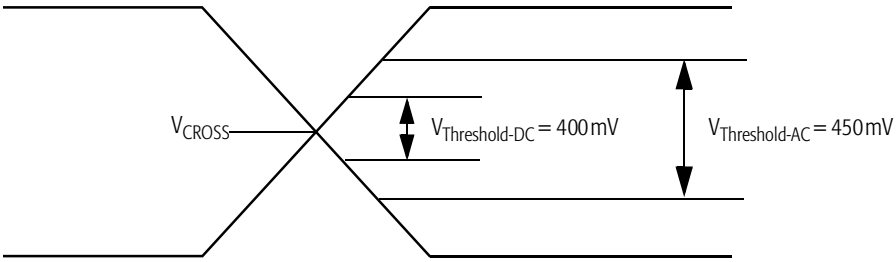


Figure 8. SYSCLK and SYSCLK# Differential Clock Signals

Table 10 shows the SYSCLK/SYSCLK# differential clock AC characteristics. Figure 9 on page 26 shows a sample waveform.

Table 10. SYSCLK and SYSCLK# AC Characteristics

Symbol	Description	Min	Max	Units	Notes
	Clock Frequency	50	100	MHz	

Notes:

1. *Circuitry driving the SYSCLK and SYSCLK# inputs must exhibit a suitably low closed-loop jitter bandwidth to allow the PLL to track the jitter. The –20 dB attenuation point, as measured into a 10-pF or 20-pF load must be less than 500 kHz.*
2. *Circuitry driving the SYSCLK and SYSCLK# inputs may purposely alter the SYSCLK and SYSCLK# period (spread spectrum clock generators). In no cases can the period violate the minimum specification above. SYSCLK and SYSCLK# inputs may vary from 100% of the specified period to 99% of the specified period at a maximum rate of 100 kHz.*

Table 10. SYSCLK and SYSCLK# AC Characteristics (continued)

Symbol	Description	Min	Max	Units	Notes
	Duty Cycle	30%	70%	–	
t_1	Period	10		ns	1, 2
t_2	High Time	4		ns	
t_3	Low Time	4		ns	
t_4	Fall Time		500	ps	
t_5	Rise Time		500	ps	
	Period Stability		± 300	ps	

Notes:

1. *Circuitry driving the SYSCLK and SYSCLK# inputs must exhibit a suitably low closed-loop jitter bandwidth to allow the PLL to track the jitter. The –20 dB attenuation point, as measured into a 10-pF or 20-pF load must be less than 500 kHz.*
2. *Circuitry driving the SYSCLK and SYSCLK# inputs may purposely alter the SYSCLK and SYSCLK# period (spread spectrum clock generators). In no cases can the period violate the minimum specification above. SYSCLK and SYSCLK# inputs may vary from 100% of the specified period to 99% of the specified period at a maximum rate of 100 kHz.*

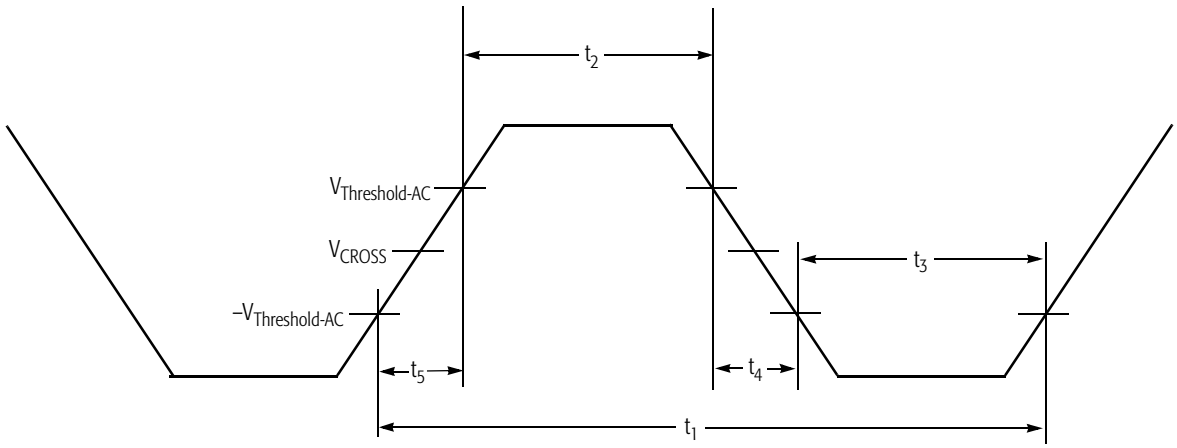


Figure 9. SYSCLK Waveform

6.10 AMD System Bus AC and DC Characteristics

Table 11 shows the DC characteristics of the AMD Athlon™ system bus used by the AMD Duron™ Processor Model 3.

Table 11. AMD System Bus DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{REF}	DC Input Reference Voltage		(0.5*VCC_CORE) –50	(0.5*VCC_CORE) +50	mV	1
$I_{VREF\_LEAK\_P}$	V_{REF} Tristate Leakage Pullup	$V_{IN} = V_{REF}$ Nominal	–100		µA	
$I_{VREF\_LEAK\_N}$	V_{REF} Tristate Leakage Pulldown	$V_{IN} = V_{REF}$ Nominal		+100	µA	
V_{IH}	Input High Voltage		V_{REF} + 200	VCC_CORE + 500	mV	
V_{IL}	Input Low Voltage		–500	V_{REF} – 200	mV	
V_{OH}	Output High Voltage	I_{OUT} = –200µA	0.85*VCC_CORE	VCC_CORE+500	mV	2
V_{OL}	Output Low Voltage	I_{OUT} = 1 mA	–500	400	mV	2
I_{LEAK_P}	Tristate Leakage Pullup	V_{IN} = VSS (Ground)	–1		mA	
I_{LEAK_N}	Tristate Leakage Pulldown	V_{IN} = VCC_CORE Nominal		+1	mA	
C_{IN}	Input Pin Capacitance		4	12	pF	3

Notes:

1. *V_{REF}:*
   – V_{REF} is nominally set by a (1%) resistor divider from VCC_CORE.
   – The suggested divider resistor values are 100 ohms over 100 ohms to produce a divisor of 0.50.
   *– Example: VCC_CORE = 1.75V, V_{REF} = 850mV (1.7 * 0.50). (Processor pin SysVrefMode = Low)*
   – Peak-to-Peak AC noise on V_{REF} (AC) should not exceed 2% of V_{REF} (DC).
2. *Specified at T = 90°C and VCC_CORE*
3. *The following processor inputs have twice the listed capacitance because they connect to two input pads— SYSCLK, and SYSCLK#. SYSCLK connects to CLKIN/RSTCLK. SYSCLK# connects to CLKIN#/RSTCLK#. For more information, see Table 16 on page 45 .*

6.11 AMD System Bus AC Characteristics

The AC characteristics of the AMD system bus are shown in Table 12. The parameters are grouped based on the source or destination of the signals involved.

Table 12. AMD System Bus AC Characteristics

Group	Symbol	Parameter	Min	Max	Units	Notes
All Signals	T_{RISE}	Output Rise Slew Rate	1	3	V/ns	1
	T_{FALL}	Output Fall Slew Rate	1	3	V/ns	1
Forward Clocks	$T_{SKEW-SAMEEDGE}$	Output skew with respect to the same clock edge		385	ps	2
	$T_{SKEW-DIFFEDGE}$	Output skew with respect to a different clock edge		770	ps	2
	T_{SU}	Input Data Setup Time	300		ps	3
	T_{HD}	Input Data Hold Time	300		ps	3
	C_{IN}	Capacitance on input Clocks	4	12	pF	
	C_{OUT}	Capacitance on output Clocks	4	12	pF	
Sync[4]	T_{VAL}	RSTCLK to Output Valid	250	2000	ps	5
	T_{SU}	Setup to RSTCLK	500		ps	6
	T_{HD}	Hold from RSTCLK	1000		ps	6

Notes:

1. *Rise and fall time ranges are guidelines over which the I/O has been characterized.*
2. *$T_{SKEW-SAMEEDGE}$ is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to the same clock edge.*
   $T_{SKEW-DIFFEDGE}$ is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to different clock edges.
3. *Input SU and HD times are with respect to the appropriate Clock Forward Group input clock.*
4. *The synchronous signals include PROCRDY, CONNECT, CLKFWDRST.*
5. *T_{VAL} is RSTCLK rising edge to output valid for PROCRDY. Test Load—25pF.*
6. *T_{SU} is setup of CONNECT/CLKFWDRST to rising edge of RSTCLK. T_{HD} is hold of CONNECT/CLKFWDRST from rising edge of RSTCLK.*

6.12 General AC and DC Characteristics

Table 13 shows the AMD Duron Processor Model 3 AC and DC characteristics of the Southbridge, JTAG, test, and miscellaneous pins.

Table 13. General AC and DC Characteristics*

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
V_{IH}	Input High Voltage		(VCC_CORE/2) + 200mV	VCC_CORE + 300mV	V	1,2
V_{IL}	Input Low Voltage		–300	350	mV	1,2
V_{OH}	Output High Voltage		VCC_CORE – 400	VCC_CORE + 300	mV	
V_{OL}	Output Low Voltage		–300	400	mV	
I_{LEAK_P}	Tristate Leakage Pullup	V_{IN} = VSS (Ground)	–1		mA	
I_{LEAK_N}	Tristate Leakage Pulldown	V_{IN} = VCC_CORE Nominal		600	µA	
I_{OH}	Output High Current			–16	mA	3
I_{OL}	Output Low Current		16		mA	3
T_{SU}	Sync Input Setup Time		2.0		ns	4, 5
T_{HD}	Sync Input Hold Time		0.0		ps	4, 5
T_{DELAY}	Output Delay with respect to RSTCLK		0.0	6.1	ns	5
T_{BIT}	Input Time to Acquire		20.0		nS	7,8

Notes:

* *These parameters were not characterized at VCC_CORE_{SLEEP}*

1. *Characterized across DC supply voltage range.*
2. *Values specified at nominal VCC_CORE. Scale parameters between VCC_CORE Min and VCC_CORE Max.*
3. *I_{OL} and I_{OH} are measured at V_{OL} max and V_{OH} min, respectively.*
4. *Synchronous inputs/outputs are specified with respect to RSTCLK and RSTCK# at the pins.*
5. *These are aggregate numbers.*
6. *Edge rates indicate the range over which inputs were characterized.*
7. *In asynchronous operation, the signal must persist for this time to guarantee capture.*
8. *This value assumes RSTCLK frequency is 10ns ⟹ TBIT = 2*fRST.*
9. *The approximate value for standard case in normal mode operation.*
10. *This value is dependent on RSTCLK frequency, divisors, LowPower mode, and core frequency.*
11. *Reassertions of the signal within this time are not guaranteed to be seen by the core.*
12. *This value assumes that the skew between RSTCLK and K7CLKOUT is much less than one phase.*
13. *This value assumes RSTCLK and K7CLKOUT are running at the same frequency, though the processor is capable of other configurations.*

Table 13. General AC and DC Characteristics* (continued)

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
T_{RPT}	Input Time to Reacquire		40.0		nS	9-13
T_{RISE}	Signal Rise Time		1.0	3.0	V/nS	6
T_{FALL}	Signal Fall Time		1.0	3.0	V/nS	6
C_{PIN}	Pin Capacitance		4	12	pF	

Notes:

* *These parameters were not characterized at VCC_CORE_{SLEEP}*

1. *Characterized across DC supply voltage range.*
2. *Values specified at nominal VCC_CORE. Scale parameters between VCC_CORE Min and VCC_CORE Max.*
3. *I_{OL} and I_{OH} are measured at V_{OL} max and V_{OH} min, respectively.*
4. *Synchronous inputs/outputs are specified with respect to RSTCLK and RSTCK# at the pins.*
5. *These are aggregate numbers.*
6. *Edge rates indicate the range over which inputs were characterized.*
7. *In asynchronous operation, the signal must persist for this time to guarantee capture.*
8. *This value assumes RSTCLK frequency is 10ns ==> TBIT = 2*fRST.*
9. *The approximate value for standard case in normal mode operation.*
10. *This value is dependent on RSTCLK frequency, divisors, LowPower mode, and core frequency.*
11. *Reassertions of the signal within this time are not guaranteed to be seen by the core.*
12. *This value assumes that the skew between RSTCLK and K7CLKOUT is much less than one phase.*
13. *This value assumes RSTCLK and K7CLKOUT are running at the same frequency, though the processor is capable of other configurations.*

6.13 APIC Pins AC and DC Characteristics

Table 14 shows the AMD Duron Processor Model 3 AC and DC characteristics of the APIC pins.

Table 14. APIC Pins AC and DC Characteristics

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
V_{IH}	Input High Voltage		1.7	2.625	V	1, 3
V_{IL}	Input Low Voltage		–300	700	mV	1, 2
V_{OH}	Output High Voltage			2.625	V	3
V_{OL}	Output Low Voltage		–300	400	mV	
I_{LEAK_P}	Tristate Leakage Pullup	V_{IN} = VSS (Ground)	–1		mA	

Notes:

1. *Characterized across DC supply voltage range*
2. *Values specified at nominal VDD (1.5 V). Scale parameters with VDD*
3. *2.625 V = 2.5 V + 5% maximum*
4. *Edge rates indicate the range over which inputs were characterized*

Table 14. APIC Pins AC and DC Characteristics (continued)

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
I_{LEAK_N}	Tristate Leakage Pulldown	V_{IN} = 2.5 V		1	mA	
I_{OL}	Output Low Current	V_{OL} Max	6		mA	
T_{RISE}	Signal Rise Time		1.0	3.0	V/nS	4
T_{FALL}	Signal Fall Time		1.0	3.0	V/nS	4
C_{PIN}	Pin Capacitance		4	12	pF	

Notes:

1. *Characterized across DC supply voltage range*
2. *Values specified at nominal VDD (1.5 V). Scale parameters with VDD*
3. *2.625 V = 2.5 V + 5% maximum*
4. *Edge rates indicate the range over which inputs were characterized*

7 Signal and Power-Up Requirements

This chapter describes the AMD Duron™ Processor Model 3 power-up requirements during system power-up and warm resets.

7.1 Power-Up Requirements

Signal Sequence and Timing Description

Figure 10 shows the relationship between key signals in the system during a power-up sequence. This figure details the requirements of the processor.

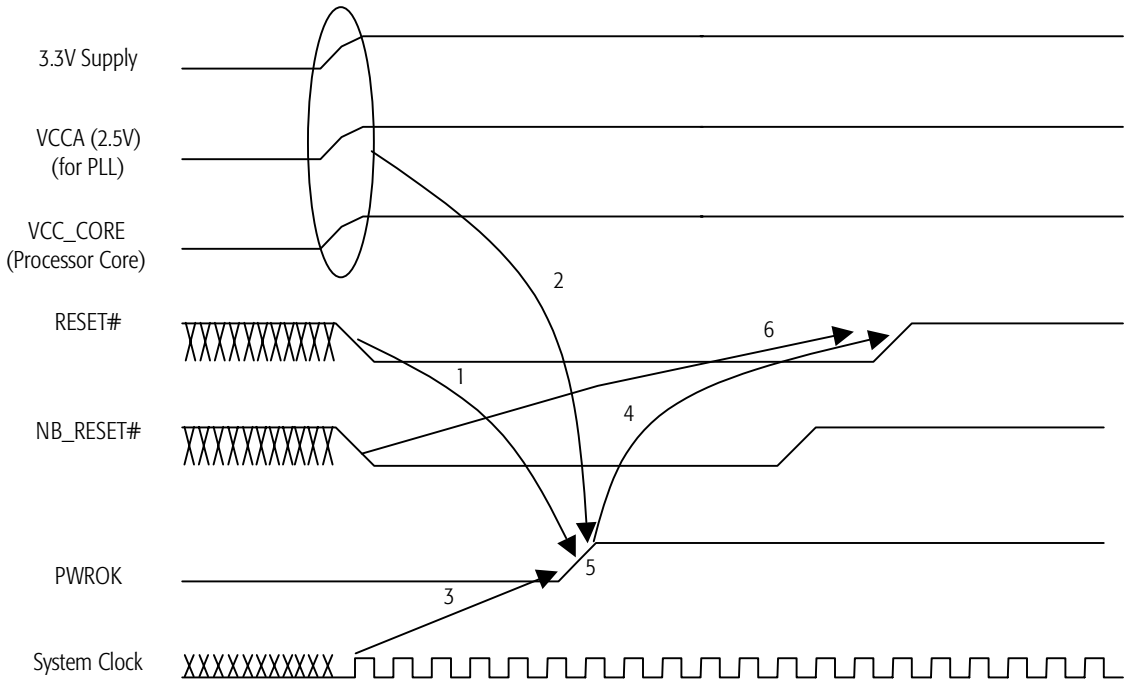


Figure 10. Signal Relationship Requirements During Power-Up Sequence

Notes: *1) Figure 10 represents several signals generically by using names not necessarily consistent with any pin lists or schematics.*

2) Requirements 1-6 in Figure 10 are described in the following section.

Power-Up Timing Requirements. The signal timing requirements are as follows:

1. RESET# must be asserted before PWROK is asserted.

   The AMD Duron Processor Model 3 does not set the correct clock multiplier if PWROK is asserted prior to a RESET# assertion. It is recommended that RESET# be asserted at least **10ns** prior to the assertion of PWROK.

   In practice, Southbridges will assert RESET# milliseconds before PWROK is deasserted.

2. All motherboard voltage planes must be within specification before PWROK is asserted.

   PWROK is an output of the voltage regulation circuit on the motherboard. PWROK indicates that VCC_CORE and all other voltage planes in the system are within specification.

   The motherboard is required to delay PWROK assertion for a minimum of 3 milliseconds from the 3.3V supply being within specification. This ensures that the system clock (SYSCLK/SYSCLK#) is operating within specification when PWROK is asserted.

   The processor core voltage, VCC_CORE, must be within specification as dictated by the VID[4:0] pins driven by the processor before PWROK is asserted. Before PWROK assertion, the AMD Athlon processor is clocked by a ring oscillator.

   The AMD Athlon processor PLL is powered by VCCA. The processor PLL does not lock if VCCA is not high enough for the processor logic to switch for some period before PWROK is asserted. VCCA must be within spec at least 5 microseconds before PWROK is asserted.

   In practice VCCA, VCC_CORE, and all other voltage planes must be within specification be for several milliseconds before PWROK is asserted.

   After PWROK is asserted, the processor PLL locks to its operational frequency.

3. The system clock (SYSCLK/SYSCLK#) must be running within specification before PWROK is asserted.

   When PWROK is asserted, the processor switches from driving the internal processor clock grid from the ring oscillator to driving from the PLL. The reference system clock should be valid at this time. The system clocks are guaranteed to be running after 3.3V has been within specification for 3 milliseconds.

4. PWROK assertion to deassertion of RESET#.

   The duration of RESET# assertion during cold boots is intended to satisfy the time it takes for the PLL to lock with a less than 1-ns phase error. The processor PLL begins to run after PWROK is asserted and the internal clock grid is switched from the ring oscillator to the PLL. The PLL lock time may take from hundreds of nanoseconds to tens of microseconds. It is recommended that the minimum time between PWROK assertion to the deassertion of RESET# be at least **1.0ms**. AMD Southbridges enforce a delay of 1.5 to 2.0 milliseconds between PWRGD (Southbridge version of PWROK) assertion and NB_RESET# deassertion.

5. PWROK must be monotonic.

   The processor should not switch between the ring oscillator and the PLL after the initial assertion of PWROK.

6. NB_RESET# must be asserted (causing CONNECT to also assert) before RESET# is deasserted. In practice all Southbridges enforce this requirement.

   If NB_RESET# does not assert until after RESET# has deasserted, the processor misinterprets the CONNECT assertion (due to NB_RESET# being asserted) as the beginning of the SIP transfer (See "Serial Initialization Packet (SIP) Protocol" on page 36). There must be sufficient overlap in the resets to ensure that CONNECT is sampled asserted by the processor before RESET# is deasserted.

Clock Multiplier Selection (FID[3:0])

When RESET# is de-asserted, the Northbridge samples the FID[3:0] Frequency ID from the processor in a chipset specific manner. For more information, see "FID[3:0] Pins" on page 62.

The Northbridge uses this FID information and other information sampled at the de-assertion of RESET# to determine the correct Serial Initialization Packet (SIP) to send to the processor for configuration of the AMD system bus for the clock multiplier(CPU frequency) indicated by the FID[3:0]

code. The SIP is sent to the processor using the SIP protocol. This protocol uses the PROCRDY, CONNECT, and CLKFWDRST signals, which are synchronous to SYSCLK.

Serial Initialization Packet (SIP) Protocol. Figure 11 shows the protocol for a typical SIP transfer to the processor after RESET# deassertion. Table 15 describes the requirements for the SIP transfer from the Northbridge to the processor. Processors and Northbridges are designed to adhere to the SIP protocol and do not require motherboard intervention.

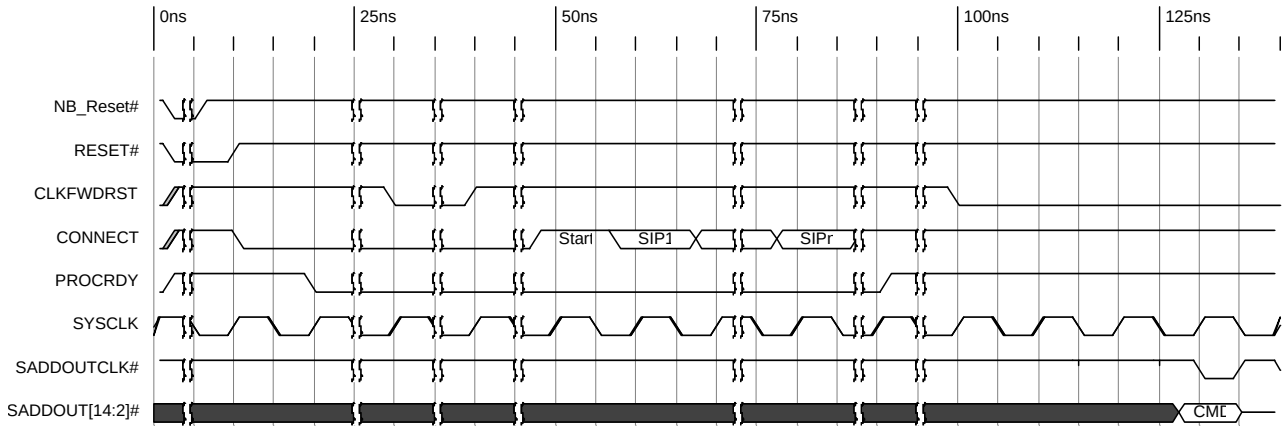


Figure 11. Typical SIP Protocol Sequence

Table 15. SIP Protocol States and Actions

State	Action
1	When NB_RESET# and RESET# are asserted, the system asserts CONNECT and CLKFWDRST and the processor asserts PROCRDY.
2	When NB_RESET# is deasserted, the system deasserts CONNECT, but continues to assert CLKFWDRST. When RESET# is deasserted, the processor deasserts PROCRDY and is ready for initialization (via the SIP Protocol). *Note: The system must be out of reset before the processor deasserts PROCRDY*
3	After one or more SYSCLK periods after the deassertion of PROCRDY, the system deasserts CLKFWDRST. (States 3 & 4 are performed for Socket A legacy reasons)
4	After one or more SYSCLK periods after the deassertion of CLKFWDRST, the system again asserts CLKFWDRST

Table 15. SIP Protocol States and Actions (continued)

<table>
<tr><th>State</th><th>Action</th></tr>
<tr><td>5</td><td>Either at the assertion of CLKFWDRST or one or more SYSCLK periods later, the processor expects the start bit (CONNECT asserted) of the SIP. The system delivers the SIP containing the processor clock-forwarding initialization state over CONNECT.
After the SIP is transferred, the system asserts and holds CONNECT. This indicates the end of the SIP transfer to the processor.</td></tr>
<tr><td>6</td><td>One or more SYSCLK periods after receiving the SIP, the processor asserts PROCRDY to indicate to the system that it has received the SIP, initialized itself, and is ready.</td></tr>
<tr><td>7</td><td>One or more SYSCLK periods after the assertion of PROCRDY, the system deasserts CLKFWDRST.</td></tr>
<tr><td>8</td><td>A number of SYSCLK periods after CLKFWDRST is sampled deasserted, the processor drives its forward clocks.
<table>
<tr><th>Processor to SYSCLK Ratio</th><th>SYSCLK Periods of Delay</th></tr>
<tr><td>3:1</td><td>3</td></tr>
<tr><td>3.5:1</td><td>3</td></tr>
<tr><td>4.0:1</td><td>3 (See Note 1)</td></tr>
<tr><td>4.5:1</td><td>3 (See Note 1)</td></tr>
<tr><td>All others</td><td>2</td></tr>
<tr><td colspan="2">Notes:
1. AMD Duron™ Processor Model 3 silicon deviates from the spec. with a 2 SysClk delay for these processor to SysClk ratios.</td></tr>
</table></td></tr>
</table>

7.2 Processor Warm Reset Requirements

The AMD Duron™ Processor Model 3 and Northbridge Reset Pins

RESET cannot be asserted to the processor without also being asserted to the Northbridge. RESET# to the Northbridge is the same in as PCI RESET#. The minimum assertion for PCI RESET# is 1 millisecond. AMD Southbridges enforce a minimum assertion of RESET#(CPU, Northbridge, PCI) of 1.5 to 2.0 milliseconds.

8 Mechanical Data

8.1 Introduction

The AMD Duron™ Processor Model 3 connects to the motherboard through a PGA socket named Socket A. For more information, see the *AMD Athlon Processor Socket 462 Application Note*, order# 90020.

8.2 Pinout Diagram

The pin location designations for the Socket A connector are shown in Figure 12 on page 40. Voided (plugged) pin locations should have a base that accepts a contact, but the top plate of Socket A should *not* have pin openings. The *exceptions* are the two plugs on the outside corners, which should be permanently closed and not accommodate a contact. It is permissible, if necessary for manufacturing reasons, to place a contact in the base at plug sites (*except* for the two plugs on the outside corners). Socket A has 462 pin sites, with 11 plugs total. For more information, see Chapter 9, "Pin Descriptions" on page 43.

In addition, Figure 12 shows the Socket A package side view and top view.

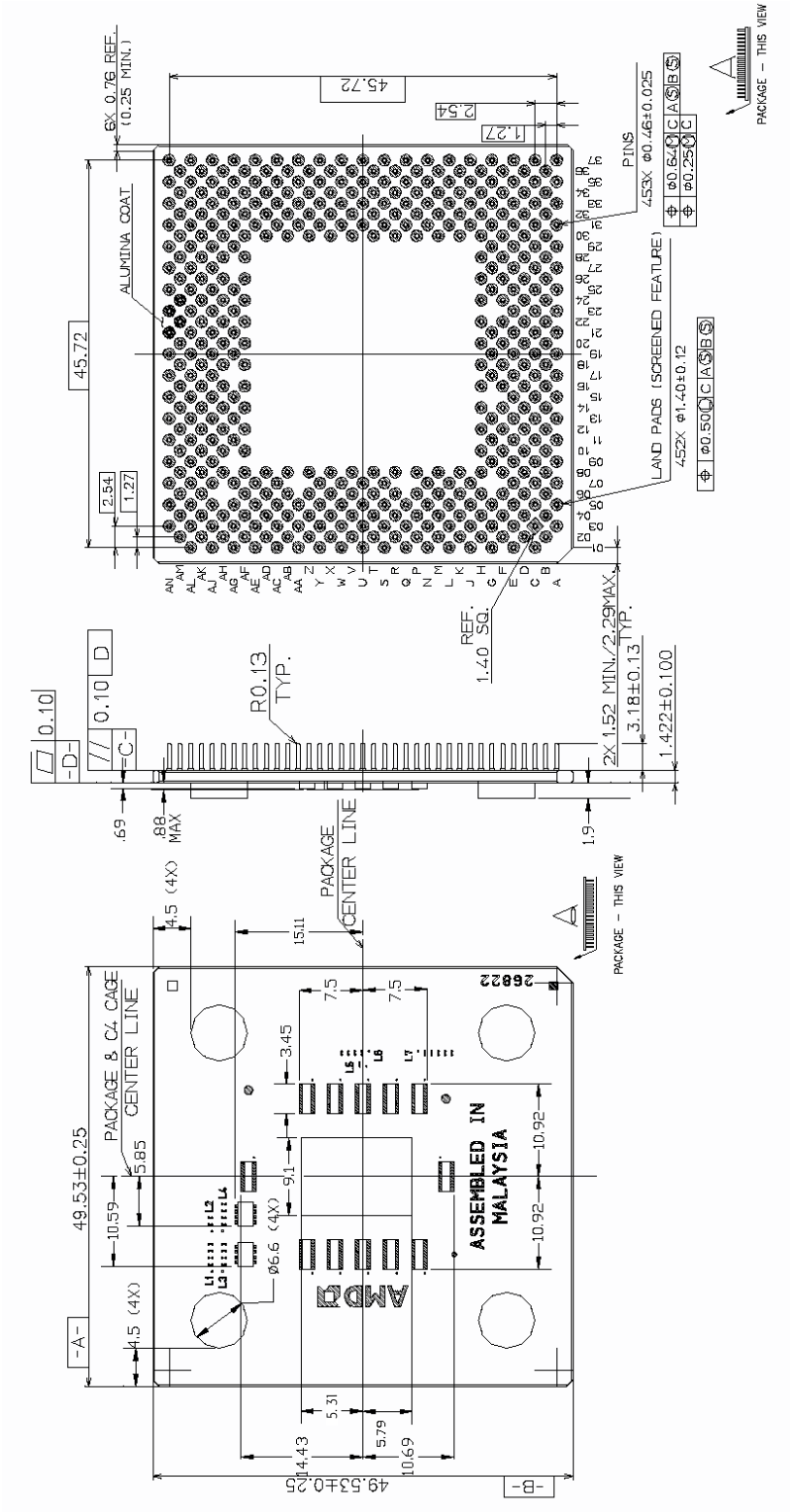
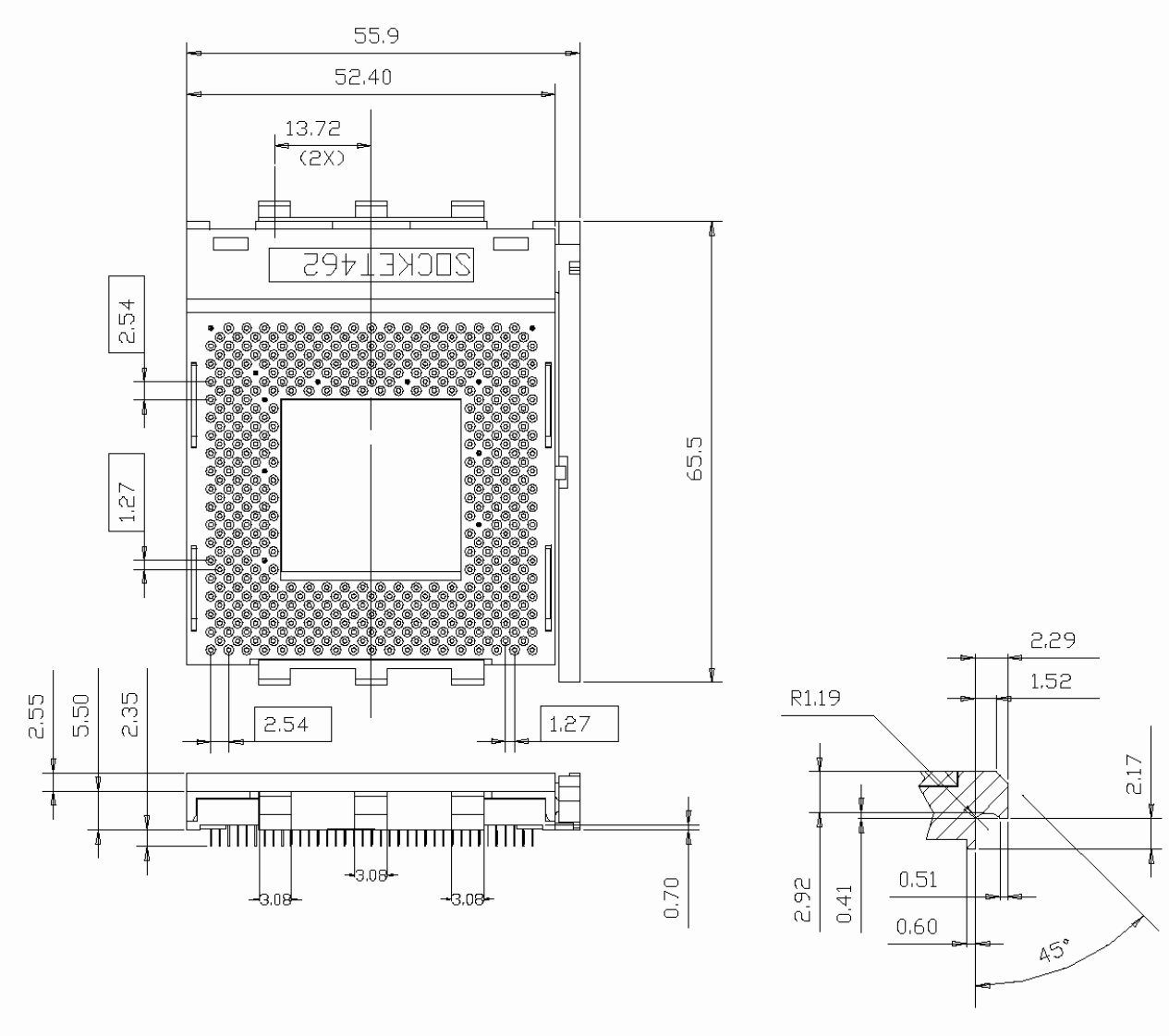


Figure 12. PGA Package, Top, Side, and Bottom Views

8.3 Socket Tabs for Heatsink Clips

Figure 13 shows the socket tab required on Socket A. These features are required to support a 300g heatsink. Figure 14 on page 42 shows the socket tab side view.



Note: *Measurements are in mm*

Figure 13. Socket A with Outline of Socket and Heatsink Tab

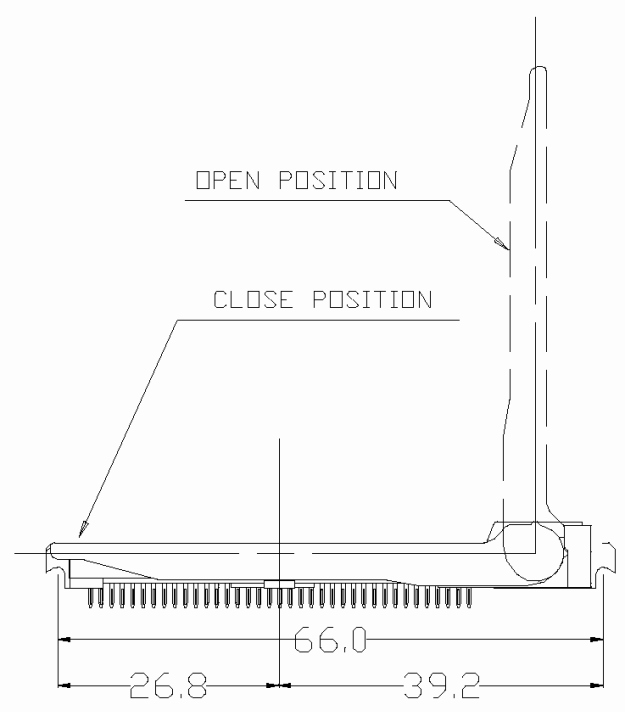


Figure 14. Socket A Heatsink Tab Side View

9 Pin Descriptions

9.1 Introduction

Figure 15 on page 44 shows the staggered pin grid array (SPGA) for the AMD Duron™ Processor Model 3. Because some of the pin names are too long to fit in the grid, they are abbreviated.

Table 16 on page 45 lists all the pins in alphabetical order by pin name, along with the abbreviation where necessary.

Table 17 on page 53 lists all the pins cross-referenced by their location.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	
A			SAO# 12		SAO#5		SAO#3		SD#55		SD#61		SD#53		SD#63		SD#62		SCK#7		SD#57		SD#39		SD#35		SD#34		SD#44		SCK#5		SDOC# 2		SD#40		SD#30	**A**
B		VSS101		VCC 100		VSS100		VCC99		VSS99		VCC98		VSS98		VCC97		VSS97		VCC96		VSS96		VCC95		VSS95		VCC94		VSS94		VCC92		VSS92		VCC91		**B**
C	SAO#7		SAO#9		SAO#8		SAO#2		SD#54		SDOC# 3		SCK#6		SD#51		SD#60		SD#59		SD#56		SD#37		SD#47		SD#38		SD#45		SD#43		SD#42		SD#41		SDOC# 1	**C**
D		VCC90		VCC89		VSS91		VCC88		VSS90		VCC87		VSS89		VCC86		VSS88		VCC85		VSS87		VCC84		VSS86		VCC82		VSS85		VCC81		VSS84		VSS83		**D**
E	SAO#11		SAO-CLK#		SAO#4		SAO#6		SD#52		SD#50		SD#49		SDIC#3		SD#48		SD#58		SD#36		SD#46		SCK#4		SDIC#2		SD#33		SD#32		SCK#3		SD#31		SD#22	**E**
F		VSS81		VSS80		VSS79		NC		VSS78		VCC80		VSS77		VCC79		VSS76		VCC78		VSS75		VCC77		VSS74		VCC76		NC		VCC75		VCC74		VCC73		**F**
G	SAO# 10		SAO# 14		SAO# 13				KEY8		NC		NC				KEY6		NC		NC				KEY4		NC		NC		NC		SD#20		SD#23		SD#21	**G**
H		VCC71		VCC70		NC		NC		NC		VCC1		VSS1		VCC2		VSS2		VCC3		VSS3		VCC4		VSS4		NC		NC		NC		VSS73		VSS72		**H**
J	SAO#0		SAO#1		NC		VID(4)																							NC		SD#19		SDIC#1		SD#29	**J**
K		VSS70		VSS69		VSS68		NC																						NC		VCC69		VCC68		VCC67		**K**
L	VID(0)		VID(1)		VID(2)		VID(3)																								NC		SD#26		SCK#2		SD#28	**L**
M		VCC66		VCC64		VCC65		VCC5																						VSS5		VSS67		VSS66		VSS65		**M**
N	PICCLK		PICD#0		PICD#1		KEY10																								NC		SD#25		SD#27		SD#18	**N**
P		VSS64		VSS63		VSS62		VSS6																						VCC6		VCC63		VCC62		VCC61		**P**
Q	TCK		TMS		SCNSN																										NC		SD#24		SD#17		SD#16	**Q**
R		VCC59		VCC58		VCC57		VCC7																						VSS7		VSS61		VSS59		VSS58		**R**
S	SCNCK1		SCNINV		SCNCK2		NC																								NC		SD#7		SD#15		SD#6	**S**
T		VSS57		VSS56		VSS55		VSS8																						VCC8		VCC56		VCC55		VCC54		**T**
U	TDI		TRST#		TDO		NC																								NC		SD#5		SD#4		SCK#0	**U**
V		VCC53		VCC52		VCC51		VCC9																						VSS9		VSS54		VSS53		VSS52		**V**
W	FID(0)		FID(1)		VREF_S		NC																								NC		SDIC#0		SD#2		SD#1	**W**
X		VSS51		VSS50		VSS48		VSS10																						VCC10		VCC50		VCC48		VCC47		**X**
Y	FID(2)		FID(3)		NC		KEY12																								NC		SCK#1		SD#3		SD#12	**Y**
Z		VCC46		VCC45		VCC44		VCC11																						VSS11		VSS47		VSS46		VSS45		**Z**
AA	DBRDY		DBREQ#		SVRFM																										NC		SD#8		SD#0		SD#13	**AA**
AB		VSS44		VSS43		VSS42		VSS12																						VCC12		VCC43		VCC42		VCC41		**AB**
AC	STPC#		PLTST#		ZN		VCC_Z																								NC		SD#10		SD#14		SD#11	**AC**
AD		VCC40		VCC39		VCC37		NC																						NC		VSS41		VSS40		VSS39		**AD**
AE	A20M#		PWROK		ZP		VSS_Z																								NC		SAI#5		SDOC# 0		SD#9	**AE**
AF		VSS38		VSS37		NC		NC		NC		VSS13		VCC13		VSS14		VCC14		VSS15		VCC15		VSS16		VCC16		NC		NC		NC		VCC36		VCC35		**AF**
AG	FERR		RESET#		NC		KEY14				COREFB		COREFB#		KEY16				NC		NC		NC		NC				KEY18		NC		SAI#2		SAI#11		SAI#7	**AG**
AH		VCC34		VCC33		AMD		NC		VCC32		VSS35		VCC31		VSS34		VCC30		VSS33		VCC29		VSS32		VCC27		VSS31		NC		VSS30		VSS29		VSS27		**AH**
AJ	IGNNE#		INIT#		VCC101		NC		NC		NC		ANLOG		NC		NC		NC		CLKFR		VCCA		PLBYP#		NC		SAI#0		SFILLV#		SAIC#		SAI#6		SAI#3	**AJ**
AK		VSS26		VSS25		VSS103		NC		VCC25		VSS23		VCC24		VSS22		VCC23		VSS21		VCC22		VSS20		VCC21		VSS19		VCC20		VSS18		VCC19		VCC18		**AK**
AL	INTR		FLUSH#		VCC26		NC		NC		NC		PLMN2		PLBYC#		CLKIN#		RCLK#		K7CO		CNNCT		NC		NC		SAI#1		SDOV#		SAI#8		SAI#4		SAI#10	**AL**
AM		VCC93		VSS102		VSS104		NC		VCC83		VSS93		VCC72		VSS82		VCC60		VSS71		VCC49		VSS60		VCC38		VSS49		VCC28		VSS28		VCC17		VSS17		**AM**
AN			NMI		SMI#		NC		NC		NC		PLMN1		PLBYC		CLKIN		RCLK		K7CO#		PRCRDY		NC		NC		SAI#12		SAI#14		SDINV#		SAI#13		SAI#9	**AN**
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	

AMD Duron™ Processor Model 3
Topside View

Figure 15. AMD Duron™ Processor Model 3 Pin Diagram—Topside View

Table 16. Pin Name Abbreviations

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
	AMD Pin	AH6			
	A20M#	AE1		NC	AE31
ANLOG	ANALOG	AJ13		NC	AG23
CLKFR	CLKFWDRESET	AJ21		NC	AG25
	CLKIN	AN17		NC	AG31
	CLKIN#	AL17		NC	AG5
CNNCT	CONNECT	AL23		NC	AJ11
	COREFB	AG11		NC	AJ15
	COREFB#	AG13		NC	AJ17
	DBRDY	AA1		NC	AJ19
	DBREQ#	AA3		NC	AJ27
	NC	AG19		NC	AL11
	NC	G21		NC	AN11
	FERR	AG1		NC	AN9
	FID[0]	W1		NC	G11
	FID[1]	W3		NC	G13
	FID[2]	Y1		NC	G27
	FID[3]	Y3		NC	G29
	FLUSH#	AL3		NC	G31
	NC	AG21		NC	J31
	NC	G19		NC	J5
	IGNNE#	AJ1		NC	L31
	INIT#	AJ3		NC	N31
	INTR	AL1		NC	Q31
K7CO	K7CLKOUT	AL21		NC	S31
K7CO#	K7CLKOUT#	AN21		NC	S7
	KEY4	G25		NC	U31
	KEY6	G17		NC	U7
	KEY8	G9		NC	W31
	KEY10	N7		NC	W7
	KEY12	Y7		NC	Y31
	KEY14	AG7		NC	Y5
	KEY16	AG15		NC	AD30
	KEY18	AG29		NC	AD8
	NC	AL25		NC	AF10
	NC	AL27		NC	AF28
	NC	AN25		NC	AF30
	NC	AN27		NC	AF32
	NC	AA31		NC	AF6

Table 16. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
	NC	AC31		NC	AF8
	NC	AH30	STPC#	STPCLK#	AC1
	NC	AH8	SAI#0	SADDIN[0]#	AJ29
	NC	AJ7	SAI#1	SADDIN[1]#	AL29
	NC	AJ9	SAI#2	SADDIN[2]#	AG33
	NC	AK8	SAI#3	SADDIN[3]#	AJ37
	NC	AL7	SAI#4	SADDIN[4]#	AL35
	NC	AL9	SAI#5	SADDIN[5]#	AE33
	NC	AM8	SAI#6	SADDIN[6]#	AJ35
	NC	AN7	SAI#7	SADDIN[7]#	AG37
	NC	F30	SAI#8	SADDIN[8]#	AL33
	NC	F8	SAI#9	SADDIN[9]#	AN37
	NC	H10	SAI#10	SADDIN[10]#	AL37
	NC	H28	SAI#11	SADDIN[11]#	AG35
	NC	H30	SAI#12	SADDIN[12]#	AN29
	NC	H32	SAI#13	SADDIN[13]#	AN35
	NC	H6	SAI#14	SADDIN[14]#	AN31
	NC	H8	SAIC#	SADDINCLK#	AJ33
	NC	K30	SAO#0	SADDOUT[0]#	J1
	NC	K8	SAO#1	SADDOUT[1]#	J3
	NMI	AN3	SAO#2	SADDOUT[2]#	C7
	PICCLK	N1	SAO#3	SADDOUT[3]#	A7
PICD#0	PICD[0]#	N3	SAO#4	SADDOUT[4]#	E5
PICD#1	PICD[1]#	N5	SAO#5	SADDOUT[5]#	A5
PLBYP#	PLLBYPASS#	AJ25	SAO#6	SADDOUT[6]#	E7
PLBYC	PLLBYPASSCLK	AN15	SAO#7	SADDOUT[7]#	C1
PLBYC#	PLLBYPASSCLK#	AL15	SAO#8	SADDOUT[8]#	C5
PLMN1	PLLMON1	AN13	SAO#9	SADDOUT[9]#	C3
PLMN2	PLLMON2	AL13	SAO#10	SADDOUT[10]#	G1
PLTST#	PLLTEST#	AC3	SAO#11	SADDOUT[11]#	E1
PRCRDY	PROCREADY	AN23	SAO#12	SADDOUT[12]#	A3
	PWROK	AE3	SAO#13	SADDOUT[13]#	G5
	RESET#	AG3	SAO#14	SADDOUT[14]#	G3
RCLK	RSTCLK	AN19	SAOCLK#	SADDOUTCLK#	E3
RCLK#	RSTCLK#	AL19	SCK#0	SCHECK[0]#	U37
SCNCK1	SCANCLK1	S1	SCK#1	SCHECK[1]#	Y33
SCNCK2	SCANCLK2	S5	SCK#2	SCHECK[2]#	L35
SCNINV	SCANINTEVAL	S3	SCK#3	SCHECK[3]#	E33
SCNSN	SCANSHIFTEN	Q5	SCK#4	SCHECK[4]#	E25

Table 16. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
	SMI#	AN5	SCK#5	SCHECK[5]#	A31
SCK#6	SCHECK[6]#	C13	SD#37	SDATA[37]#	C23
SCK#7	SCHECK[7]#	A19	SD#38	SDATA[38]#	C27
SD#0	SDATA[0]#	AA35	SD#39	SDATA[39]#	A23
SD#1	SDATA[1]#	W37	SD#40	SDATA[40]#	A35
SD#2	SDATA[2]#	W35	SD#41	SDATA[41]#	C35
SD#3	SDATA[3]#	Y35	SD#42	SDATA[42]#	C33
SD#4	SDATA[4]#	U35	SD#43	SDATA[43]#	C31
SD#5	SDATA[5]#	U33	SD#44	SDATA[44]#	A29
SD#6	SDATA[6]#	S37	SD#45	SDATA[45]#	C29
SD#7	SDATA[7]#	S33	SD#46	SDATA[46]#	E23
SD#8	SDATA[8]#	AA33	SD#47	SDATA[47]#	C25
SD#9	SDATA[9]#	AE37	SD#48	SDATA[48]#	E17
SD#10	SDATA[10]#	AC33	SD#49	SDATA[49]#	E13
SD#11	SDATA[11]#	AC37	SD#50	SDATA[50]#	E11
SD#12	SDATA[12]#	Y37	SD#51	SDATA[51]#	C15
SD#13	SDATA[13]#	AA37	SD#52	SDATA[52]#	E9
SD#14	SDATA[14]#	AC35	SD#53	SDATA[53]#	A13
SD#15	SDATA[15]#	S35	SD#54	SDATA[54]#	C9
SD#16	SDATA[16]#	Q37	SD#55	SDATA[55]#	A9
SD#17	SDATA[17]#	Q35	SD#56	SDATA[56]#	C21
SD#18	SDATA[18]#	N37	SD#57	SDATA[57]#	A21
SD#19	SDATA[19]#	J33	SD#58	SDATA[58]#	E19
SD#20	SDATA[20]#	G33	SD#59	SDATA[59]#	C19
SD#21	SDATA[21]#	G37	SD#60	SDATA[60]#	C17
SD#22	SDATA[22]#	E37	SD#61	SDATA[61]#	A11
SD#23	SDATA[23]#	G35	SD#62	SDATA[62]#	A17
SD#24	SDATA[24]#	Q33	SD#63	SDATA[63]#	A15
SD#25	SDATA[25]#	N33	SDIC#0	SDATAINCLK[0]#	W33
SD#26	SDATA[26]#	L33	SDIC#1	SDATAINCLK[1]#	J35
SD#27	SDATA[27]#	N35	SDIC#2	SDATAINCLK[2]#	E27
SD#28	SDATA[28]#	L37	SDIC#3	SDATAINCLK[3]#	E15
SD#29	SDATA[29]#	J37	SDINV#	SDATAINVALID#	AN33
SD#30	SDATA[30]#	A37	SDOC#0	SDATAOUTCLK[0]#	AE35
SD#31	SDATA[31]#	E35	SDOC#1	SDATAOUTCLK[1]#	C37
SD#32	SDATA[32]#	E31	SDOC#2	SDATAOUTCLK[2]#	A33
SD#33	SDATA[33]#	E29	SDOC#3	SDATAOUTCLK[3]#	C11
SD#34	SDATA[34]#	A27	SDOV#	SDATAOUTVALID#	AL31
SD#35	SDATA[35]#	A25	SFILLV#	SFILLVAL#	AJ31

Table 16. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
SD#36	SDATA[36]#	E21	SVRFM	SYSVREFMODE	AA5
	TCK	Q1	VCC35	VCC_CORE35	AF36
	TDI	U1	VCC36	VCC_CORE36	AF34
	TDO	U5	VCC37	VCC_CORE37	AD6
	TMS	Q3	VCC38	VCC_CORE38	AM26
	TRST#	U3	VCC39	VCC_CORE39	AD4
VCC1	VCC_CORE1	H12	VCC40	VCC_CORE40	AD2
VCC2	VCC_CORE2	H16	VCC41	VCC_CORE41	AB36
VCC3	VCC_CORE3	H20	VCC42	VCC_CORE42	AB34
VCC4	VCC_CORE4	H24	VCC43	VCC_CORE43	AB32
VCC5	VCC_CORE5	M8	VCC44	VCC_CORE44	Z6
VCC6	VCC_CORE6	P30	VCC45	VCC_CORE45	Z4
VCC7	VCC_CORE7	R8	VCC46	VCC_CORE46	Z2
VCC8	VCC_CORE8	T30	VCC47	VCC_CORE47	X36
VCC9	VCC_CORE9	V8	VCC48	VCC_CORE48	X34
VCC10	VCC_CORE10	X30	VCC49	VCC_CORE49	AM22
VCC11	VCC_CORE11	Z8	VCC50	VCC_CORE50	X32
VCC12	VCC_CORE12	AB30	VCC51	VCC_CORE51	V6
VCC13	VCC_CORE13	AF14	VCC52	VCC_CORE52	V4
VCC14	VCC_CORE14	AF18	VCC53	VCC_CORE53	V2
VCC15	VCC_CORE15	AF22	VCC54	VCC_CORE54	T36
VCC16	VCC_CORE16	AF26	VCC55	VCC_CORE55	T34
VCC17	VCC_CORE17	AM34	VCC56	VCC_CORE56	T32
VCC18	VCC_CORE18	AK36	VCC57	VCC_CORE57	R6
VCC19	VCC_CORE19	AK34	VCC58	VCC_CORE58	R4
VCC20	VCC_CORE20	AK30	VCC59	VCC_CORE59	R2
VCC21	VCC_CORE21	AK26	VCC60	VCC_CORE60	AM18
VCC22	VCC_CORE22	AK22	VCC61	VCC_CORE61	P36
VCC23	VCC_CORE23	AK18	VCC62	VCC_CORE62	P34
VCC24	VCC_CORE24	AK14	VCC63	VCC_CORE63	P32
VCC25	VCC_CORE25	AK10	VCC64	VCC_CORE64	M4
VCC26	VCC_CORE26	AL5	VCC65	VCC_CORE65	M6
VCC27	VCC_CORE27	AH26	VCC66	VCC_CORE66	M2
VCC28	VCC_CORE28	AM30	VCC67	VCC_CORE67	K36
VCC29	VCC_CORE29	AH22	VCC68	VCC_CORE68	K34
VCC30	VCC_CORE30	AH18	VCC69	VCC_CORE69	K32
VCC31	VCC_CORE31	AH14	VCC70	VCC_CORE70	H4
VCC32	VCC_CORE32	AH10	VCC71	VCC_CORE71	H2
VCC33	VCC_CORE33	AH4	VCC72	VCC_CORE72	AM14

Table 16. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
VCC34	VCC_CORE34	AH2	VCC73	VCC_CORE73	F36
VCC74	VCC_CORE74	F34		VSS100	B6
VCC75	VCC_CORE75	F32		VSS101	B2
VCC76	VCC_CORE76	F28		VSS102	AM4
VCC77	VCC_CORE77	F24		VSS103	AK6
VCC78	VCC_CORE78	F20		VSS104	AM6
VCC79	VCC_CORE79	F16		VSS11	Z30
VCC80	VCC_CORE80	F12		VSS12	AB8
VCC81	VCC_CORE81	D32		VSS13	AF12
VCC82	VCC_CORE82	D28		VSS14	AF16
VCC83	VCC_CORE83	AM10		VSS15	AF20
VCC84	VCC_CORE84	D24		VSS16	AF24
VCC85	VCC_CORE85	D20		VSS17	AM36
VCC86	VCC_CORE86	D16		VSS18	AK32
VCC87	VCC_CORE87	D12		VSS19	AK28
VCC88	VCC_CORE88	D8		VSS2	H18
VCC89	VCC_CORE89	D4		VSS20	AK24
VCC90	VCC_CORE90	D2		VSS21	AK20
VCC91	VCC_CORE91	B36		VSS22	AK16
VCC92	VCC_CORE92	B32		VSS23	AK12
VCC93	VCC_CORE93	AM2		VSS25	AK4
VCC94	VCC_CORE94	B28		VSS26	AK2
VCC95	VCC_CORE95	B24		VSS27	AH36
VCC96	VCC_CORE96	B20		VSS28	AM32
VCC97	VCC_CORE97	B16		VSS29	AH34
VCC98	VCC_CORE98	B12		VSS3	H22
VCC99	VCC_CORE99	B8		VSS30	AH32
VCC100	VCC_CORE100	B4		VSS31	AH28
VCC101	VCC_CORE101	AJ5		VSS32	AH24
	VCC_Z	AC7		VSS33	AH20
	VCCA	AJ23		VSS34	AH16
	VID[0]	L1		VSS35	AH12
	VID[1]	L3		VSS37	AF4
	VID[2]	L5		VSS38	AF2
	VID[3]	L7		VSS39	AD36
	VID[4]	J7		VSS4	H26
VREF_S	VREF_SYS	W5		VSS40	AD34
	VSS_Z	AE7		VSS41	AD32
	VSS1	H14		VSS42	AB6

Table 16. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
	VSS10	X8		VSS43	AB4
	VSS44	AB2		VSS8	T8
	VSS45	Z36		VSS80	F4
	VSS46	Z34		VSS81	F2
	VSS47	Z32		VSS82	AM16
	VSS48	X6		VSS83	D36
	VSS49	AM28		VSS84	D34
	VSS5	M30		VSS85	D30
	VSS50	X4		VSS86	D26
	VSS51	X2		VSS87	D22
	VSS52	V36		VSS88	D18
	VSS53	V34		VSS89	D14
	VSS54	V32		VSS9	V30
	VSS55	T6		VSS90	D10
	VSS56	T4		VSS91	D6
	VSS57	T2		VSS92	B34
	VSS58	R36		VSS93	AM12
	VSS59	R34		VSS94	B30
	VSS6	P8		VSS95	B26
	VSS60	AM24		VSS96	B22
	VSS61	R32		VSS97	B18
	VSS62	P6		VSS98	B14
	VSS63	P4		VSS99	B10
	VSS64	P2		ZN	AC5
	VSS65	M36		ZP	AE5

Table 16. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
	VSS66	M34			
	VSS67	M32			
	VSS68	K6			
	VSS69	K4			
	VSS7	R30			
	VSS70	K2			
	VSS71	AM20			
	VSS72	H36			
	VSS73	H34			
	VSS74	F26			
	VSS75	F22			
	VSS76	F18			
	VSS77	F14			
	VSS78	F10			
	VSS79	F6			

9.2 Pin List

Table 17 cross-references the Socket A pin location to the signal name.

The “L” (Level) column shows the electrical specification for this pin. “P” indicates a push-pull mode driven by a single source. “O” indicates open drain mode that allows devices to share the pin.

Note: *The Socket A AMD Duron Processor Model 3 supports push-pull drivers. For more information, see “Push-Pull (PP) Drivers” on page 6.*

The “P” (Port) column indicates if this signal is an input (I), output (O), or bidirectional (B) signal.

The “R” (Reference) column indicates if this clock-forwarded signal should be referenced to the VSS (G) or VCC_CORE (P) planes for the purpose of providing proper current return paths for the signal routes. For more information, see the *Socket A Motherboard Design Guide*, order# 24363.

The Description column contains a cross-reference to a page with more information in the “Detailed Pin Descriptions“ (which starts on page 60).

Table 17. Socket A Pin Cross-Reference by Pin Location

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
A1	No Pin	Page 64	-	-	-	B2	VSS		-	-	-
A3	SADDOUT[12]#		P	O	G	B4	VCC_CORE		-	-	-
A5	SADDOUT[5]#		P	O	G	B6	VSS		-	-	-
A7	SADDOUT[3]#		P	O	G	B8	VCC_CORE		-	-	-
A9	SDATA[55]#		P	B	P	B10	VSS		-	-	-
A11	SDATA[61]#		P	B	P	B12	VCC_CORE		-	-	-
A13	SDATA[53]#		P	B	G	B14	VSS		-	-	-
A15	SDATA[63]#		P	B	G	B16	VCC_CORE		-	-	-
A17	SDATA[62]#		P	B	G	B18	VSS		-	-	-
A19	SCHECK[7]#	Page 64	P	B	G	B20	VCC_CORE		-	-	-
A21	SDATA[57]#		P	B	G	B22	VSS		-	-	-
A23	SDATA[39]#		P	B	G	B24	VCC_CORE		-	-	-
A25	SDATA[35]#		P	B	P	B26	VSS		-	-	-
A27	SDATA[34]#		P	B	P	B28	VCC_CORE		-	-	-
A29	SDATA[44]#		P	B	G	B30	VSS		-	-	-
A31	SCHECK[5]#	Page 64	P	B	G	B32	VCC_CORE		-	-	-
A33	SDATAOUTCLK[2]#		P	O	P	B34	VSS		-	-	-
A35	SDATA[40]#		P	B	G	B36	VCC_CORE		-	-	-
A37	SDATA[30]#		P	B	P						
C1	SADDOUT[7]#		P	O	G	D2	VCC_CORE		-	-	-
C3	SADDOUT[9]#		P	O	G	D4	VCC_CORE		-	-	-
C5	SADDOUT[8]#		P	O	G	D6	VSS		-	-	-
C7	SADDOUT[2]#		P	O	G	D8	VCC_CORE		-	-	-
C9	SDATA[54]#		P	B	P	D10	VSS		-	-	-
C11	SDATAOUTCLK[3]#		P	O	G	D12	VCC_CORE		-	-	-
C13	SCHECK[6]#	Page 64	P	B	G	D14	VSS		-	-	-
C15	SDATA[51]#		P	B	P	D16	VCC_CORE		-	-	-
C17	SDATA[60]#		P	B	G	D18	VSS		-	-	-
C19	SDATA[59]#		P	B	G	D20	VCC_CORE		-	-	-
C21	SDATA[56]#		P	B	G	D22	VSS		-	-	-
C23	SDATA[37]#		P	B	P	D24	VCC_CORE		-	-	-
C25	SDATA[47]#		P	B	G	D26	VSS		-	-	-
C27	SDATA[38]#		P	B	G	D28	VCC_CORE		-	-	-
C29	SDATA[45]#		P	B	G	D30	VSS		-	-	-

Table 17. Socket A Pin Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
C31	SDATA[43]#		P	B	G	D32	VCC_CORE		-	-	-
C33	SDATA[42]#		P	B	G	D34	VSS		-	-	-
C35	SDATA[41]#		P	B	G	D36	VSS		-	-	-
C37	SDATAOUTCLK[1]#		P	O	G						
E1	SADDOUT[11]#		P	O	P	F2	VSS		-	-	-
E3	SADDOUTCLK#		P	O	G	F4	VSS		-	-	-
E5	SADDOUT[4]#		P	O	P	F6	VSS		-	-	-
E7	SADDOUT[6]#		P	O	G	F8	NC Pin	Page 63	-	-	-
E9	SDATA[52]#		P	B	P	F10	VSS		-	-	-
E11	SDATA[50]#		P	B	P	F12	VCC_CORE		-	-	-
E13	SDATA[49]#		P	B	G	F14	VSS		-	-	-
E15	SDATAINCLK[3]#		P	I	G	F16	VCC_CORE		-	-	-
E17	SDATA[48]#		P	B	P	F18	VSS		-	-	-
E19	SDATA[58]#		P	B	G	F20	VCC_CORE		-	-	-
E21	SDATA[36]#		P	B	P	F22	VSS		-	-	-
E23	SDATA[46]#		P	B	P	F24	VCC_CORE		-	-	-
E25	SCHECK[4]#	Page 64	P	B	P	F26	VSS		-	-	-
E27	SDATAINCLK[2]#		P	I	G	F28	VCC_CORE		-	-	-
E29	SDATA[33]#		P	B	P	F30	NC Pin	Page 63	-	-	-
E31	SDATA[32]#		P	B	P	F32	VCC_CORE		-	-	-
E33	SCHECK[3]#	Page 64	P	B	P	F34	VCC_CORE		-	-	-
E35	SDATA[31]#		P	B	P	F36	VCC_CORE		-	-	-
E37	SDATA[22]#		P	B	G						
G1	SADDOUT[10]#		P	O	P	H2	VCC_CORE		-	-	-
G3	SADDOUT[14]#		P	O	G	H4	VCC_CORE		-	-	-
G5	SADDOUT[13]#		P	O	G	H6	NC Pin	Page 63	-	-	-
G7	Key Pin	Page 63	-	-	-	H8	NC Pin	Page 63	-	-	-
G9	Key Pin	Page 63	-	-	-	H10	NC Pin	Page 63	-	-	-
G11	NC Pin	Page 63	-	-	-	H12	VCC_CORE		-	-	-
G13	NC Pin	Page 63	-	-	-	H14	VSS		-	-	-
G15	Key Pin	Page 63	-	-	-	H16	VCC_CORE		-	-	-
G17	Key Pin	Page 63	-	-	-	H18	VSS		-	-	-
G19	NC Pin	Page 63	-	-	-	H20	VCC_CORE		-	-	-
G21	NC Pin	Page 63	-	-	-	H22	VSS		-	-	-

Table 17. Socket A Pin Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
G23	Key Pin	Page 63	-	-	-	H24	VCC_CORE		-	-	-
G25	Key Pin	Page 63	-	-	-	H26	VSS		-	-	-
G27	NC Pin	Page 63	-	-	-	H28	NC Pin	Page 63	-	-	-
G29	NC Pin	Page 63	-	-	-	H30	NC Pin	Page 63	-	-	-
G31	NC Pin	Page 63	-	-	-	H32	NC Pin	Page 63	-	-	-
G33	SDATA[20]#		P	B	G	H34	VSS		-	-	-
G35	SDATA[23]#		P	B	G	H36	VSS		-	-	-
G37	SDATA[21]#		P	B	G						
J1	SADDOUT[0]#	Page 64	P	O	-	K2	VSS		-	-	-
J3	SADDOUT[1]#	Page 64	P	O	-	K4	VSS		-	-	-
J5	NC Pin	Page 63	-	-	-	K6	VSS		-	-	-
J7	VID[4]	Page 65	O	O	-	K8	NC Pin	Page 63	-	-	-
J31	NC Pin	Page 63	-	-	-	K30	NC Pin	Page 63	-	-	-
J33	SDATA[19]#		P	B	G	K32	VCC_CORE		-	-	-
J35	SDATAINCLK[1]#		P	I	P	K34	VCC_CORE		-	-	-
J37	SDATA[29]#		P	B	P	K36	VCC_CORE		-	-	-
L1	VID[0]	Page 65	O	O	-	M2	VCC_CORE		-	-	-
L3	VID[1]	Page 65	O	O	-	M4	VCC_CORE		-	-	-
L5	VID[2]	Page 65	O	O	-	M6	VCC_CORE		-	-	-
L7	VID[3]	Page 65	O	O	-	M8	VCC_CORE		-	-	-
L31	NC Pin	Page 63	-	-	-	M30	VSS		-	-	-
L33	SDATA[26]#		P	B	P	M32	VSS		-	-	-
L35	SCHECK[2]#	Page 64	P	B	G	M34	VSS		-	-	-
L37	SDATA[28]#		P	B	P	M36	VSS		-	-	-
N1	PICCLK		O	I	-	P2	VSS		-	-	-
N3	PICD[0]#		O	B	-	P4	VSS		-	-	-
N5	PICD[1]#		O	B	-	P6	VSS		-	-	-
N7	Key Pin	Page 63	-	-	-	P8	VSS		-	-	-
N31	NC Pin	Page 63	-	-	-	P30	VCC_CORE		-	-	-
N33	SDATA[25]#		P	B	P	P32	VCC_CORE		-	-	-
N35	SDATA[27]#		P	B	P	P34	VCC_CORE		-	-	-
N37	SDATA[18]#		P	B	G	P36	VCC_CORE		-	-	-
Q1	TCK	Page 63	P	I	-	R2	VCC_CORE		-	-	-
Q3	TMS	Page 63	P	I	-	R4	VCC_CORE		-	-	-

Table 17. Socket A Pin Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
Q5	SCANSHIFTEN	Page 64	P	I	-	R6	VCC_CORE		-	-	-
Q7	Key Pin	Page 63	-	-	-	R8	VCC_CORE		-	-	-
Q31	NC Pin	Page 63	-	-	-	R30	VSS		-	-	-
Q33	SDATA[24]#		P	B	P	R32	VSS		-	-	-
Q35	SDATA[17]#		P	B	G	R34	VSS		-	-	-
Q37	SDATA[16]#		P	B	G	R36	VSS		-	-	-
S1	SCANCLK1	Page 64	P	I	-	T2	VSS		-	-	-
S3	SCANINTEVAL	Page 64	P	I	-	T4	VSS		-	-	-
S5	SCANCLK2	Page 64	P	I	-	T6	VSS		-	-	-
S7	NC Pin	Page 63	-	-	-	T8	VSS		-	-	-
S31	NC Pin	Page 63	-	-	-	T30	VCC_CORE		-	-	-
S33	SDATA[7]#		P	B	G	T32	VCC_CORE		-	-	-
S35	SDATA[15]#		P	B	P	T34	VCC_CORE		-	-	-
S37	SDATA[6]#		P	B	G	T36	VCC_CORE		-	-	-
U1	TDI	Page 63	P	I	-	V2	VCC_CORE		-	-	-
U3	TRST#	Page 63	P	I	-	V4	VCC_CORE		-	-	-
U5	TDO	Page 63	P	O	-	V6	VCC_CORE		-	-	-
U7	NC Pin	Page 63	-	-	-	V8	VCC_CORE		-	-	-
U31	NC Pin	Page 63	-	-	-	V30	VSS		-	-	-
U33	SDATA[5]#		P	B	G	V32	VSS		-	-	-
U35	SDATA[4]#		P	B	G	V34	VSS		-	-	-
U37	SCHECK[0]#	Page 64	P	B	G	V36	VSS		-	-	-
W1	FID[0]	Page 62	O	-	-	X2	VSS		-	-	-
W3	FID[1]	Page 62	O	-	-	X4	VSS		-	-	-
W5	VREFSYS	Page 66	P	-	-	X6	VSS		-	-	-
W7	NC Pin	Page 63	-	-	-	X8	VSS		-	-	-
W31	NC Pin	Page 63	-	-	-	X30	VCC_CORE		-	-	-
W33	SDATAINCLK[0]#		P	I	G	X32	VCC_CORE		-	-	-
W35	SDATA[2]#		P	B	G	X34	VCC_CORE		-	-	-
W37	SDATA[1]#		P	B	P	X36	VCC_CORE		-	-	-
Y1	FID[2]	Page 62	O	-	-	Z2	VCC_CORE		-	-	-
Y3	FID[3]	Page 62	O	-	-	Z4	VCC_CORE		-	-	-
Y5	NC Pin	Page 63	-	-	-	Z6	VCC_CORE		-	-	-
Y7	Key Pin	Page 63	-	-	-	Z8	VCC_CORE		-	-	-

Table 17. Socket A Pin Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
Y31	NC Pin	Page 63	-	-	-	Z30	VSS		-	-	-
Y33	SCHECK[1]#	Page 64	P	B	P	Z32	VSS		-	-	-
Y35	SDATA[3]#		P	B	G	Z34	VSS		-	-	-
Y37	SDATA[12]#		P	B	P	Z36	VSS		-	-	-
AA1	DBRDY	Page 61	P	O	-	AB2	VSS		-	-	-
AA3	DBREQ#	Page 61	P	I	-	AB4	VSS		-	-	-
AA5	SYSVREFMODE	Page 65	P	I	-	AB6	VSS		-	-	-
AA7	Key Pin	Page 63	-	-	-	AB8	VSS		-	-	-
AA31	NC Pin	Page 63	-	-	-	AB30	VCC_CORE		-	-	-
AA33	SDATA[8]#		P	B	P	AB32	VCC_CORE		-	-	-
AA35	SDATA[0]#		P	B	G	AB34	VCC_CORE		-	-	-
AA37	SDATA[13]#		P	B	G	AB36	VCC_CORE		-	-	-
AC1	STPCLK#	Page 65	P	I	-	AD2	VCC_CORE		-	-	-
AC3	PLLTEST#	Page 64	P	I	-	AD4	VCC_CORE		-	-	-
AC5	ZN	Page 66	P	-	-	AD6	VCC_CORE		-	-	-
AC7	VCC_Z	Page 66	-	-	-	AD8	NC Pin	Page 63	-	-	-
AC31	NC Pin	Page 63	-	-	-	AD30	NC Pin	Page 63	-	-	-
AC33	SDATA[10]#		P	B	P	AD32	VSS		-	-	-
AC35	SDATA[14]#		P	B	G	AD34	VSS		-	-	-
AC37	SDATA[11]#		P	B	G	AD36	VSS		-	-	-
AE1	A20M#	Page 60	P	I	-	AE31	NC Pin	Page 63	-	-	-
AE3	PWROK	Page 64	P	I	-	AE33	SADDIN[5]#		P	I	G
AE5	ZP	Page 66	P	-	-	AE35	SDATAOUTCLK[0]#		P	O	P
AE7	VSS_Z	Page 66	-	-	-	AE37	SDATA[9]#		P	B	G
AF2	VSS		-	-	-	AG1	FERR	Page 61	-	O	-
AF4	VSS		-	-	-	AG3	RESET#		-	I	-
AF6	NC Pin	Page 63	-	-	-	AG5	NC Pin	Page 63	-	-	-
AF8	NC Pin	Page 63	-	-	-	AG7	Key Pin	Page 63	-	-	-
AF10	NC Pin	Page 63	-	-	-	AG9	Key Pin	Page 63	-	-	-
AF12	VSS		-	-	-	AG11	COREFB	Page 60	-	-	-
AF14	VCC_CORE		-	-	-	AG13	COREFB#	Page 60	-	-	-
AF16	VSS		-	-	-	AG15	Key Pin	Page 63	-	-	-
AF18	VCC_CORE		-	-	-	AG17	Key Pin	Page 63	-	-	-
AF20	VSS		-	-	-	AG19	NC Pin	Page 63	-	-	-

Table 17. Socket A Pin Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
AF22	VCC_CORE		-	-	-	AG21	NC Pin	Page 63	-	-	-
AF24	VSS		-	-	-	AG23	NC Pin	Page 63	-	-	-
AF26	VCC_CORE		-	-	-	AG25	NC Pin	Page 63	-	-	-
AF28	NC Pin	Page 63	-	-	-	AG27	Key Pin	Page 63	-	-	-
AF30	NC Pin	Page 63	-	-	-	AG29	Key Pin	Page 63	-	-	-
AF32	NC Pin	Page 63	-	-	-	AG31	NC Pin	Page 63	-	-	-
AF34	VCC_CORE		-	-	-	AG33	SADDIN[2]#		P	I	G
AF36	VCC_CORE		-	-	-	AG35	SADDIN[11]#		P	I	G
						AG37	SADDIN[7]#		P	I	P
AH2	VCC_CORE		-	-	-	AJ1	IGNNE#	Page 63	P	I	-
AH4	VCC_CORE		-	-	-	AJ3	INIT#	Page 63	P	I	-
AH6	AMD Pin	Page 60	-	-	-	AJ5	VCC_CORE		-	-	-
AH8	NC Pin	Page 63	-	-	-	AJ7	NC Pin	Page 63	-	-	-
AH10	VCC_CORE		-	-	-	AJ9	NC Pin	Page 63	-	-	-
AH12	VSS		-	-	-	AJ11	NC Pin	Page 63	-	-	-
AH14	VCC_CORE		-	-	-	AJ13	Analog	Page 60	-	-	-
AH16	VSS		-	-	-	AJ15	NC Pin	Page 63	-	-	-
AH18	VCC_CORE		-	-	-	AJ17	NC Pin	Page 63	-	-	-
AH20	VSS		-	-	-	AJ19	NC Pin	Page 63	-	-	-
AH22	VCC_CORE		-	-	-	AJ21	CLKFWDRST	Page 60	P	I	P
AH24	VSS		-	-	-	AJ23	VCCA	Page 65	-	-	-
AH26	VCC_CORE		-	-	-	AJ25	PLLBYPASS#	Page 64	P	I	-
AH28	VSS		-	-	-	AJ27	NC Pin	Page 63	-	-	-
AH30	NC Pin	Page 63	-	-	-	AJ29	SADDIN[0]#	Page 64	-	-	-
AH32	VSS		-	-	-	AJ31	SFILLVAL#		P	I	G
AH34	VSS		-	-	-	AJ33	SADDINCLK#		P	I	G
AH36	VSS		-	-	-	AJ35	SADDIN[6]#		P	I	P
						AJ37	SADDIN[3]#		P	I	G
AK2	VSS		-	-	-	AL1	INTR	Page 63	P	I	-
AK4	VSS		-	-	-	AL3	FLUSH#	Page 63	P	I	-
AK6	VSS		-	-	-	AL5	VCC_CORE		-	-	-
AK8	NC Pin	Page 63	-	-	-	AL7	NC Pin	Page 63	-	-	-
AK10	VCC_CORE		-	-	-	AL9	NC Pin	Page 63	-	-	-
AK12	VSS		-	-	-	AL11	NC Pin	Page 63	-	-	-

Table 17. Socket A Pin Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
AK14	VCC_CORE		-	-	-	AL13	PLLMON2	Page 64	O	O	-
AK16	VSS		-	-	-	AL15	PLLBYPASSCLK#	Page 64	P	I	-
AK18	VCC_CORE		-	-	-	AL17	CLKIN#	Page 60	P	I	P
AK20	VSS		-	-	-	AL19	RSTCLK#	Page 60	P	I	P
AK22	VCC_CORE		-	-	-	AL21	K7CLKOUT	Page 63	P	O	-
AK24	VSS		-	-	-	AL23	CONNECT	Page 60	P	I	P
AK26	VCC_CORE		-	-	-	AL25	NC Pin	Page 63	-	-	-
AK28	VSS		-	-	-	AL27	NC Pin	Page 63	-	-	-
AK30	VCC_CORE		-	-	-	AL29	SADDIN[1]#	Page 64	P	I	-
AK32	VSS		-	-	-	AL31	SDATAOUTVAL#		P	O	P
AK34	VCC_CORE		-	-	-	AL33	SADDIN[8]#		P	I	P
AK36	VCC_CORE		-	-	-	AL35	SADDIN[4]#		P	I	G
						AL37	SADDIN[10]#		P	I	G
AM2	VCC_CORE		-	-	-	AN1	No Pin	Page 64	-	-	-
AM4	VSS		-	-	-	AN3	NMI	Page 64	P	I	-
AM6	VSS		-	-	-	AN5	SMI#	Page 64	P	I	-
AM8	NC Pin	Page 63	-	-	-	AN7	NC Pin	Page 63	-	-	-
AM10	VCC_CORE		-	-	-	AN9	NC Pin	Page 63	-	-	-
AM12	VSS		-	-	-	AN11	NC Pin	Page 63	-	-	-
AM14	VCC_CORE		-	-	-	AN13	PLLMON1	Page 64	O	B	-
AM16	VSS		-	-	-	AN15	PLLBYPASSCLK	Page 64	P	I	-
AM18	VCC_CORE		-	-	-	AN17	CLKIN	Page 60	-	I	P
AM20	VSS		-	-	-	AN19	RSTCLK	Page 60	-	I	P
AM22	VCC_CORE		-	-	-	AN21	K7CLKOUT#	Page 63	P	O	-
AM24	VSS		-	-	-	AN23	PROCRDY		-	O	P
AM26	VCC_CORE		-	-	-	AN25	NC Pin	Page 63	-	-	-
AM28	VSS		-	-	-	AN27	NC Pin	Page 63	-	-	-
AM30	VCC_CORE		-	-	-	AN29	SADDIN[12]#		P	I	G
AM32	VSS		-	-	-	AN31	SADDIN[14]#		P	I	G
AM34	VCC_CORE		-	-	-	AN33	SDATAINVAL#		P	I	P
AM36	VSS		-	-	-	AN35	SADDIN[13]#		P	I	G
						AN37	SADDIN[9]#		P	I	G

9.3 Detailed Pin Descriptions

The information in this section pertains to Table 17 on page 53. For specific resistor values, see the *Socket A Motherboard Design Guide*, order# 24363.

A20M# Pin

A20M# is an input from the system used to simulate address wrap-around in the 20-bit 8086.

AMD Pin

The motherboard should treat the AMD pin (AH6) as an NC pin. A socket designer has the option of creating a top mold piece that blocks this pin location. However, sockets that populate the AMD pin must be allowed, so the motherboard must always provide for a NC type pin at this pin location. AMD Socket A s do not implement a pin at location AH6. When a socket that does not provide a pin hole at location AH6 is used, a non-AMD PGA370 part does not fit into Socket A.

AMD System Bus Pins

See the *AMD System Bus Specification*, order# 21902 for information about the system bus pins—PROCRDY, PWROK, RESET#, SADDIN[14:2]#, SADDINCLK#, SADDOUT[14:2]#, SADDOUTCLK#, SCHECK[7:0]#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAINVAL#, SDATAOUTCLK[3:0]#, SDATAOUTVAL#, SFILLVAL#.

Analog Pin

Treat this pin as an NC.

CLKFWDRST Pin

CLKFWDRST resets clock-forward circuitry for both the system and processor.

CLKIN, RSTCLK (SYSCLK) Pins

Connect CLKIN (AN17) with RSTCLK (AN19) and name it SYSCLK. Connect CLKIN# (AL17) with RSTCLK# (AL19) and name it SYSCLK#. Length match the clocks from the clock generator to the Northbridge and processor. See “SYSCLK and SYSCLK# Pins” on page 65 for more information.

CONNECT Pin

CONNECT is an input from the system used for power management and clock-forward initialization at reset.

COREFB and COREFB# Pins

COREFB and COREFB# are outputs to the system that provide AMD Duron Processor Model 3 core voltage feedback to the system.

DBRDY and DBREQ# Pins

DBRDY (AA1) and DBREQ# (AA3) are routed to the debug connector. DBREQ# is tied to VCC_CORE with a pullup resistor.

FERR Pin

FERR is an output to the system that is asserted for any unmasked numerical exception independent of the NE bit in CR0. FERR is an open drain active High signal that must be inverted and level shifted to an active Low signal. For more information about FERR and FERR#, see the "Required Circuits" chapter of the *Socket A Motherboard Design Guide*, order# 24363.

FID[3:0] Pins

See "Frequency Identification (FID[3:0])" on page 22 for the AC and DC characteristics for FID[3:0].

FID[3] (Y3), FID[2] (Y1), FID[1] (W3), and FID[0] (W1) are the 4-bit processor clock-to-SYSCLK ratio. Table 18 describes the encodings of the clock multipliers on FID[3:0].

Table 18. FID[3:0] Clock Multiplier Encodings

FID[3]	FID[2]	FID[1]	FID[0]	Processor Clock to SYSCLK Frequency Ratio
0	0	0	0	11
0	0	0	1	11.5
0	0	1	0	12
0	0	1	1	>= 12.5
0	1	0	0	5
0	1	0	1	5.5
0	1	1	0	6
0	1	1	1	6.5
1	0	0	0	7
1	0	0	1	7.5
1	0	1	0	8
1	0	1	1	8.5
1	1	0	0	9
1	1	0	1	9.5
1	1	1	0	10
1	1	1	1	10.5

Note:
All ratios greater than or equal to 12.5x have the same FID[3:0] code of 0011, which causes the SIP configuration for all ratios of 12.5x or greater to be the same.

The FID[3:0] signals are open drain processor outputs that are pulled High on the motherboard and sampled by the Northbridge at the deassertion of RESET# to determine the SIP (serialization initialization packet) that gets sent to the processor. See the *AMD System Bus Specification*, order#21902 for more information about the SIP and SIP protocol.

The processor FID[3:0] outputs are open drain and 2.5V tolerant. **To prevent damage to the processor, if these signals are pulled High to above 2.5 V, they must be electrically isolated from the processor.** For information about the FID[3:0] isolation circuit, see the *Socket A Motherboard Design Guide*, order# 24363.

FLUSH# Pin To the debug connector, this pin should be tied to VCC_CORE with a pullup resistor, and to SMI# with a resistor that is not populated.

IGNNE# Pin IGNNE# is an input from the system that tells the processor to ignore numeric errors.

INIT# Pin INIT# is an input from the system that resets the integer registers without affecting the floating-point registers or the internal caches. Execution starts at 0FFFF FFF0h.

INTR Pin INTR is an input from the system that causes the processor to start an interrupt acknowledge transaction that fetches the 8-bit interrupt vector and starts execution at that location.

JTAG Pins TCK (Q1), TMS (Q3), TDI (U1), TRST# (U3), and TDO (U5) are the JTAG interface. Connect these pins directly to the motherboard debug connector. Pullup TDI, TCK, TMS, and TRST# to VCC_CORE.

K7CLKOUT and K7CLKOUT# Pins K7CLKOUT (AL21) and K7CLKOUT# (AN21) are each run for 2 to 3 inches and then terminated with a resistor pair, 100 ohms to VCC_CORE and 100 ohms to VSS. The effective termination resistance and voltage are 50 ohms and VCC_CORE/2.

Key Pins These 16 locations are for processor type keying for forwards and backwards compatibility (G7, G9, G15, G17, G23, G25, N7, Q7, Y7, AA7, AG7, AG9, AG15, AG17, AG27, and AG29). Motherboard designers should treat key pins like NC (no connect) pins. See “NC Pins” on page 63 for more information. A socket designer has the option of creating a top mold piece that allows PGA key pins only where designated. However, sockets that populate all key pins must be allowed, so the motherboard must always provide for pins at all 16 key pin locations.

NC Pins The motherboard should provide a plated hole for an NC pin. The pin hole should not be electrically connected to anything.

NMI Pin

NMI is an input from the system that causes a non-maskable interrupt.

PGA Orientation Pins

No pin is present at pin locations A1 and AN1 (see the *Processor Socket 462 Application Note*, order# 90020). Motherboard designers should not allow for a PGA socket pin at these locations.

PLL Bypass and Test Pins

PLLTEST# (AC3), PLLMON1 (AN13), PLLMON2 (AL13), PLLBYPASSCLK (AN15), and PLLBYPASSCLK# (AL15) are the PLL bypass and test interface. This interface is tied disabled on the motherboard. All six pin signals are routed to the debug connector. All four processor inputs (PLLTEST#, PLLMON1, and PLLMON2) are tied to VCC_CORE with pullup resistors.

PWROK Pin

Motherboard designs require power sequencing circuitry for processor PLL startup protection. PLL startup complications can occur if PWROK is asserted before the following voltages are valid:

- VCC_CORE
- PLL voltage
- 3.3-V supply, which indicates the system clocks are stable.

For more information, see the "Motherboard Required Circuits" chapter of the *Socket A Motherboard Design Guide*, order# 24363.

SADDIN[1]# and SADDOUT[1:0]# Pins

SADDIN[1]# is tied to VSS with pulldown resistors, if this bit is not supported by the Northbridge. SADDOUT[1:0]# are NC, if these bits are not supported by the Northbridge. For more information, see the *AMD System Bus Specification*, order# 21902.

Scan Pins

SCANSHIFTEN (Q5), SCANCLK1 (S1), SCANINTEVAL (S3), and SCANCLK2 (S5) are the scan interface. This interface is AMD internal and is disabled with a pulldown resistor to VSS on the motherboard.

SCHECK[7:0]# Pin

For systems that do not support ECC, SCHECK[7:0]# should be treated as NC pins.

SMI# Pin

SMI# is an input that causes the processor to enter the system management mode.

STPCLK# Pin

STPCLK# is an input that causes the processor to enter a lower power mode and issue a Stop Grant special cycle.

SYSCLK and SYSCLK# Pins

SYSCLK and SYSCLK# are differential input clock signals provided to the processor's PLL from a system-clock generator. See "CLKIN, RSTCLK (SYSCLK) Pins" on page 60 for more information.

SYSVREFMODE Pin

SYSVREFMODE (AA5) is Low to ensure that the external VREFSYS voltage is the actual voltage used by the input buffers and that no scaling occurs internally between the VREFSYS voltage and the input threshold. This pin is tied Low with a pulldown resistor, which is required to enable Push-Pull system bus functionality.

VCCA Pin

VCCA is the processor PLL supply. VCCA current ranges from 0 mA to 32 mA at ~1 GHz. Vmax is 2.75 V and Vmin is 2.25 V. Decouple this pin with a 0.1-uF capacitor. For information about the VCCA pin, see Table 5, "VCCA AC and DC Characteristics," on page 23 and the "Motherboard Required Circuits" chapter of the *Socket A Motherboard Design Guide*, order# 24363.

VID[4:0] Pins

The VID[4:0] signals are outputs to the motherboard that indicate the required VCC_CORE voltage for the processor. The VCC_CORE ID (VID) is sent to the motherboard VCC_CORE regulator. The processor VID[4:0] outputs are open drain. See "Voltage Identification (VID[4:0])" on page 22 for the AC and DC characteristics for VID[4:0].

The motherboard is required to pull VID[4:0] High for the voltage regulator to supply voltage in the appropriate range for the AMD Duron Processor Model 3. These voltage ID values are defined inTable 19 on page 66.

Note: *The VID[3:0] for Slot A has a different code definition than VID[4:0] for Socket A.*

Table 19. VID[4:0] Code to Voltage Definition

VID[4:0]	VCC_CORE (V)	VID[4:0]	VCC_CORE (V)
00000	1.850	10000	1.450
00001	1.825	10001	1.425
00010	1.800	10010	1.400
00011	1.775	10011	1.375
00100	1.750	10100	1.350
00101	1.725	10101	1.325
00110	1.700	10110	1.300
00111	1.675	10111	1.275
01000	1.650	11000	1.250
01001	1.625	11001	1.225
01010	1.600	11010	1.200
01011	1.575	11011	1.175
01100	1.550	11100	1.150
01101	1.525	11101	1.125
01110	1.500	11110	1.100
01111	1.475	11111	No CPU

For more information, see the "Required Circuits" chapter of the *Socket A Motherboard Design Guide*, order# 24363.

VREFSYS Pin

VREFSYS (W5) drives the threshold voltage for the system bus input receivers. VREFSYS is set to 0.5 * VCC_CORE. In addition, to minimize VCC_CORE noise rejection from VREFSYS, include decoupling capacitors. For more information, see the *Socket A Motherboard Design Guide*, order# 24363.

ZN, VCC_Z, ZP, and VSS_Z Pins

ZN (AC5), VCC_Z (AC7), ZP (AE5), and VSS_Z (AE7) are the push-pull compensation circuit pins. VCC_Z is tied to VCC_CORE. VSS_Z is tied to VSS.

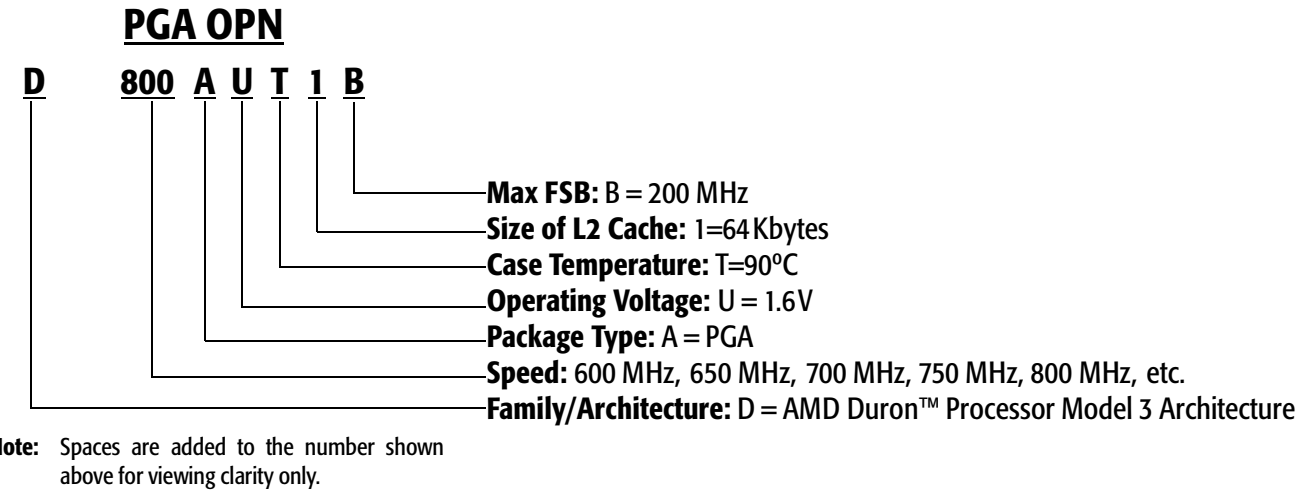
If Push-Pull mode is selected by the SIP parameter SysPushPull asserted (SysPushPull=1), ZN is tied to VCC_CORE with a resistor that has a resistance matching the impedance Zo of the transmission line. ZP is tied to VSS with a resistor that has a resistance matching the impedance Zo of the transmission line.

If Open-Drain mode is selected by the SIP parameter SysPushPull deasserted (SysPushPull=0), ZN and ZP should be resistively tied to either VCC_CORE or VSS, but should not be left floating.

10 Ordering Information

Standard AMD Duron™ Processor Model 3 Products

AMD standard products are available in several operating ranges. The ordering part numbers (OPN) are formed by a combination of the elements shown in Figure 16. ***These OPNs are examples only.***



Note: Spaces are added to the number shown above for viewing clarity only.

Figure 16. PGA OPN Example for the AMD Duron™ Processor Model 3

Appendix A

Conventions, Abbreviations, and References

This section contains information about the conventions and abbreviations used in this document.

Signals and Bits

- Active-Low Signals—Signal names containing a pound sign, such as SFILL#, indicate active-Low signals. They are asserted in their Low-voltage state and negated in their High-voltage state. When used in this context, High and Low are written with an initial upper case letter.
- Signal Ranges—In a range of signals, the highest and lowest signal numbers are contained in brackets and separated by a colon (for example, D[63:0]).
- Reserved Bits and Signals—Signals or bus bits marked *reserved* must be driven inactive or left unconnected, as indicated in the signal descriptions. These bits and signals are reserved by AMD for future implementations. When software reads registers with reserved bits, the reserved bits must be masked. When software writes such registers, it must first read the register and change only the non-reserved bits before writing back to the register.
- Three-State—In timing diagrams, signal ranges that are high impedance are shown as a straight horizontal line half-way between the high and low levels.

- Invalid and Don't-Care—In timing diagrams, signal ranges that are invalid or don't-care are filled with a screen pattern.

Data Terminology

The following list defines data terminology:

- Quantities
  - A *word* is two bytes (16 bits)
  - A *doubleword* is four bytes (32 bits)
  - A *quadword* is eight bytes (64 bits)
- Addressing—Memory is addressed as a series of bytes on eight-byte (64-bit) boundaries in which each byte can be separately enabled.
- Abbreviations—The following notation is used for bits and bytes:
  - Kilo (K, as in 4-Kbyte page)
  - Mega (M, as in 4 Mbits/sec)
  - Giga (G, as in 4 Gbytes of memory space)

  See Table 21 for more abbreviations.
- Little-Endian Convention—The byte with the address xx...xx00 is in the least-significant byte position (little end). In byte diagrams, bit positions are numbered from right to left—the little end is on the right and the big end is on the left. Data structure diagrams in memory show low addresses at the bottom and high addresses at the top. When data items are aligned, bit notation on a 64-bit data bus maps directly to bit notation in 64-bit-wide memory. Because byte addresses increase from right to left, strings appear in reverse order when illustrated.
- Bit Ranges—In text, bit ranges are shown with a dash (for example, bits 9–1). When accompanied by a signal or bus name, the highest and lowest bit numbers are contained in brackets and separated by a colon (for example, AD[31:0]).
- Bit Values—Bits can either be set to 1 or cleared to 0.
- Hexadecimal and Binary Numbers—Unless the context makes interpretation clear, hexadecimal numbers are followed by an h and binary numbers are followed by a b.

Abbreviations and Acronyms

Table 21 contains the definitions of abbreviations used in this document.

Table 20. Abbreviations

Abbreviation	Meaning
A	Ampere
F	Farad
G	Giga-
Gbit	Gigabit
Gbyte	Gigabyte
H	Henry
h	Hexadecimal
K	Kilo-
Kbyte	Kilobyte
M	Mega-
Mbit	Megabit
Mbyte	Megabyte
MHz	Megahertz
m	Milli-
ms	Millisecond
mW	Milliwatt
μ	Micro-
μA	Microampere
μF	Microfarad
μH	Microhenry
μs	Microsecond
μV	Microvolt
n	nano-
nA	nanoampere
nF	nanofarad
nH	nanohenry
ns	nanosecond
ohm	Ohm
p	pico-
pA	picoampere

Table 20. Abbreviations (continued)

Abbreviation	Meaning
pF	picofarad
pH	picohenry
ps	picosecond
s	Second
V	Volt
W	Watt

Table 21 contains the definitions of acronyms used in this document.

Table 21. Acronyms

Abbreviation	Meaning
ACPI	Advanced Configuration and Power Interface
AGP	Accelerated Graphics Port
APCI	AGP Peripheral Component Interconnect
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
BIOS	Basic Input/Output System
BIST	Built-In Self-Test
BIU	Bus Interface Unit
DDR	Double-Data Rate
DIMM	Dual Inline Memory Module
DMA	Direct Memory Access
DRAM	Direct Random Access Memory
ECC	Error Correcting Code
EIDE	Enhanced Integrated Device Electronics
EISA	Extended Industry Standard Architecture
EPROM	Enhanced Programmable Read Only Memory
EV6	Digital™ Alpha™ Bus
FIFO	First In, First Out
GART	Graphics Address Remapping Table
HSTL	High-Speed Transistor Logic
IDE	Integrated Device Electronics
ISA	Industry Standard Architecture

Table 21. Acronyms (continued)

Abbreviation	Meaning
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LAN	Large Area Network
LRU	Least-Recently Used
LVTTL	Low Voltage Transistor Transistor Logic
MSB	Most Significant Bit
MTRR	Memory Type and Range Registers
MUX	Multiplexer
NMI	Non-Maskable Interrupt
OD	Open-Drain
PBGA	Plastic Ball Grid Array
PA	Physical Address
PCI	Peripheral Component Interconnect
PDE	Page Directory Entry
PDT	Page Directory Table
PLL	Phase Locked Loop
PMSM	Power Management State Machine
POS	Power-On Suspend
POST	Power-On Self-Test
RAM	Random Access Memory
ROM	Read Only Memory
RXA	Read Acknowledge Queue
SDI	System DRAM Interface
SDRAM	Synchronous Direct Random Access Memory
SIP	Serial Initialization Packet
SMbus	System Management Bus
SPD	Serial Presence Detect
SRAM	Synchronous Random Access Memory
SROM	Serial Read Only Memory
TLB	Translation Lookaside Buffer
TOM	Top of Memory
TTL	Transistor Transistor Logic
VAS	Virtual Address Space
VPA	Virtual Page Address

Table 21. Acronyms (continued)

Abbreviation	Meaning
VGA	Video Graphics Adapter
USB	Universal Serial Bus
ZDB	Zero Delay Buffer