HOT-557
Layout-Version 1.5
Pentium™ processor
Based PCI MAIN BOARD

User's Manual

FCC Notice:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy. If not installed and used properly, in strict accordance with the manufacturer's instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures :

Reorient or relocate the receiving antenna.

Increase the separation between the equipment and receiver.

Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

Consult the dealer or an experienced radio/television technician for help and for additional suggestions.

The user may find the following booklet prepared by the Federal Communications Commission helpful "How to Identify and Resolve Radio-TV Interference Problems." This booklet is available from the U.S. Government Printing Office. Washington, DC 20402, Stock 004-000-00345-4

FCC Warning

The user is cautioned that changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

Note : In order for an installation of this product to maintain compliance with the limits for a Class B device, shielded cables and power cord must be used.

CE Notice:

Following standards were applied to this product, in order to achieve compliance with the electromagnetic compatibility:

- Immunity in accordance with EN 50082-1: 1992
- Emmitions in accordance with EN 55022: 1987 Class B.

NOTICE

Manual Ver 3.4

All information, documentation, and specifications contained in this manual are subject to change without prior notification by the manufacturer.

The author assumes no responsibility for any errors or omissions which may appear in this document nor does it make a commitment to update the information contained herein.

TRADEMARKS

Intel is a registered trademark of Intel Corporation

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PS/2 is a registered trademark of IBM Corporation.

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TABLE OF CONTENTS

Preface

HOT-557 mainboard is a highly integrated IBM PC/AT compatible system board. The design will accept Intel Pentium, Cyrix/IBM 6x86/L and AMD K5 / K6 processors and also features high-performance pipeline burst secondary cache memory support with size of 256KB and 512KB. The memory subsystem is designed to support up to 128 MB of EDO RAM, Standard Fast Page DRAM and SDRAM in standard 72-pin SIMM socket and 168-pin 3.3 V DIMM socket. A type 7 Pentium processor socket provides access to future processor enhancements.

HOT-557 provides a new level of I/O integration. Intel's 82430VX PCIset chipset provides increased integration and improved performance over other chipset designs. The 82430VX PCIset chipset provides an integrated Bus Mastering IDE controller with two high performance IDE interfaces for up to four IDE devices.

The onboard Super I/O controller provides the standard PC I/O functions: floppy interface, two FIFO serial ports, an IrDA device port and a SPP/EPP/ ECP capable parallel port.

Up to four PCI local bus slots provide a high bandwidth data path for data-movement intensive functions such as graphics, and up to three ISA slots complete the I/O function.

The HOT-557 provides the foundation for cost effective, high performance, highly expandable platforms, which deliver the latest in Pentium processor and I/O standard

Chapter 1 Introduction

Specification

CPU Function

- Pentium processors P54C : 75~200 MHz
- Pentium processors P55C (MMX) : 166~233 MHz
- Cyrix/IBM 6x86/L processors : P120+~P166+
- AMD K5 processors : PR75~PR200
- AMD K6 processors : PR2-166~PR2-233

Chipset

- Intel PCIset 82437VX, 82438VX and 82371SB

Memory

- Supports two banks of EDO, Fast Page Mode DRAM or 3.3V Sync. DRAM ranging from 8MB to 128MB
- Supports 4MB, 8MB, 16MB, 32MB 72-pins SIMMs or 8MB, 16MB, 32MB 168-pin DIMMs

Cache Memory

- Integrated L2 write-back cache controller

  - 256KB or 512KB Direct Mapped Pipeline Burst Cache

Power Management Function

- Provides four power management modes : Full on, Doze, Standby, and Suspend
- Supports Microsoft APM
- Provides EPMI (External Power Management Interrupt) pin

Expansions

- 32-bit PCI bus slot x 4
- 16-bit ISA bus slot x 3
- 2-channel PCI IDE port
  - Support up to 4 IDE devices
  - PIO Mode 4, DMA Mode 2 transfers up to 22 MB/sec
  - Integrated 8 x 32-bit buffer for PCI IDE burst transfers
- One floppy port
- One parallel port
  - Supports **SPP** (PS/2 compatible bidirectional Parallel Port), **EPP** (Enhanced Parallel Port), and **ECP** (Extended Capabilities Port) high performance parallel port.
- Two serial ports
  - Supports 16C550 compatible UARTS.
  - Supports IrDA (Infra-red) communication.
- One PS/2 mouse port
- Two USB (Universal Serial Bus) ports

System Bios

- Award PnP Bios v4.51PG
  Bundled with Symbios Login (NCR) SDCM V4.0 SCSI Bios

Board Design

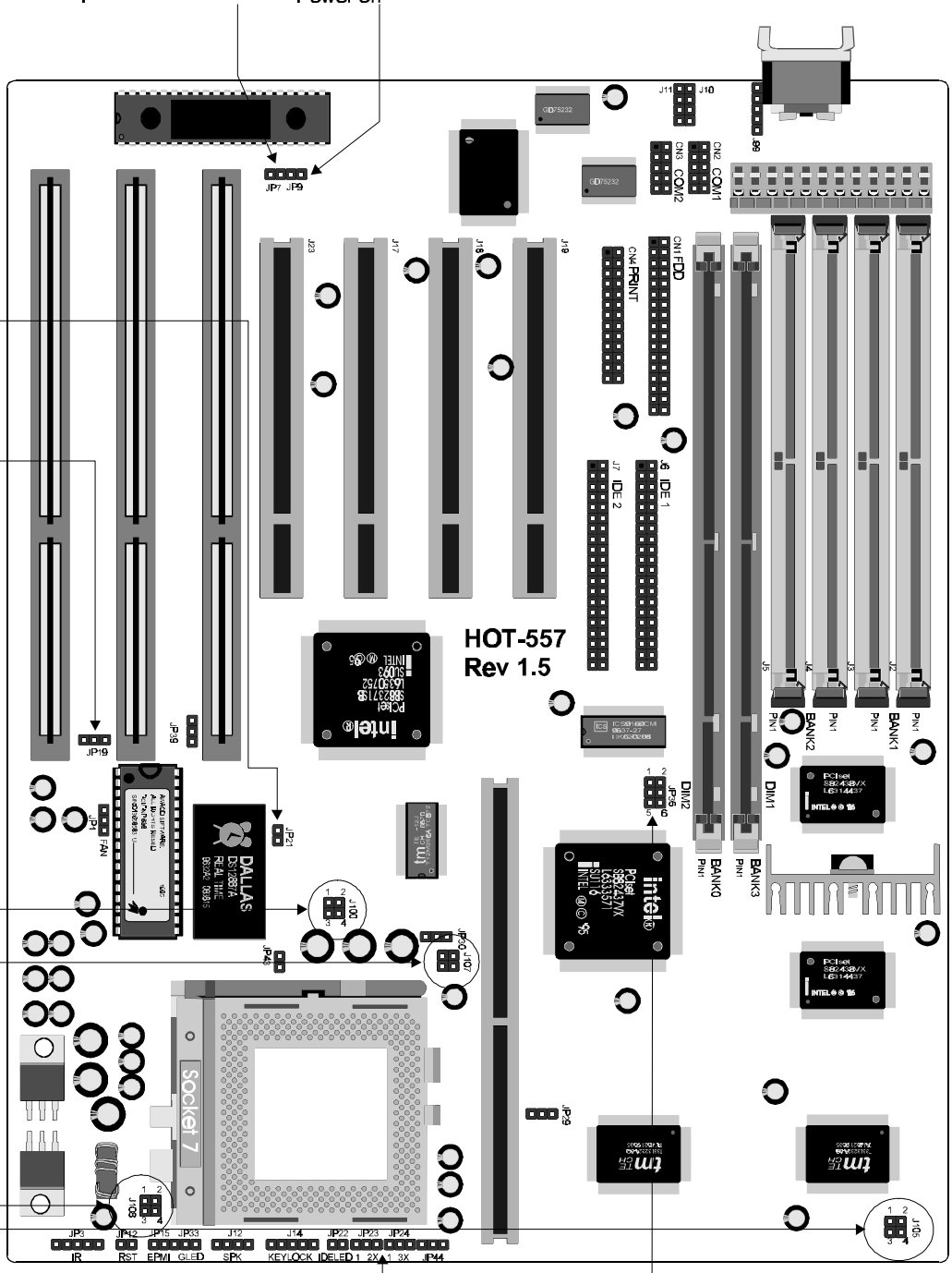
- Dimension 220mm x 280mm

Chapter 2 Hardware Configuration

Jumpers

JP7 Display Type Switch
Close : EGA/CGA
Open : Monochrome

JP9 Clear Password,
Close Jumper during Power on



JP21 CMOS Clear
Close : Clear CMOS
Open : Normal

JP19, Flash EPROM Vpp Select

	JP19
5V	2 - 3
12V	1 - 2

CPU Voltage Select-1
VIO=VCORE
J107 - All Open,
J108 - Pin 1-3,2-4 Close,

J100

3.53V	1-3, 2-4 Close
3.33V	1-3 Close
3.10V	3-4 Close
2.94V	2-4 Close
2.82V	All Open

CPU Voltage Select-2
VIO, VCORE Separate
J107 - Pin 1-3, 2-4 Close
J108 - All Open,

VIO - J105

3.44V	2-4 Close
3.33V	3-4 Close

VCORE - J00

2.82V	All Open
2.94V	2-3 Close
3.10V	3-4 Close

CPU Clock Multiplier Select - JP23, JP24

	JP23	JP24
1 : 1.5	Pin 2-3 close	Pin 2-3 close
1 : 2	Pin 1-2 close	Pin 2-3 close
1 : 3	Pin 2-3 close	Pin 1-2 close
1 : 2.5/1.75	Pin 1-2 close	Pin 1-2 close

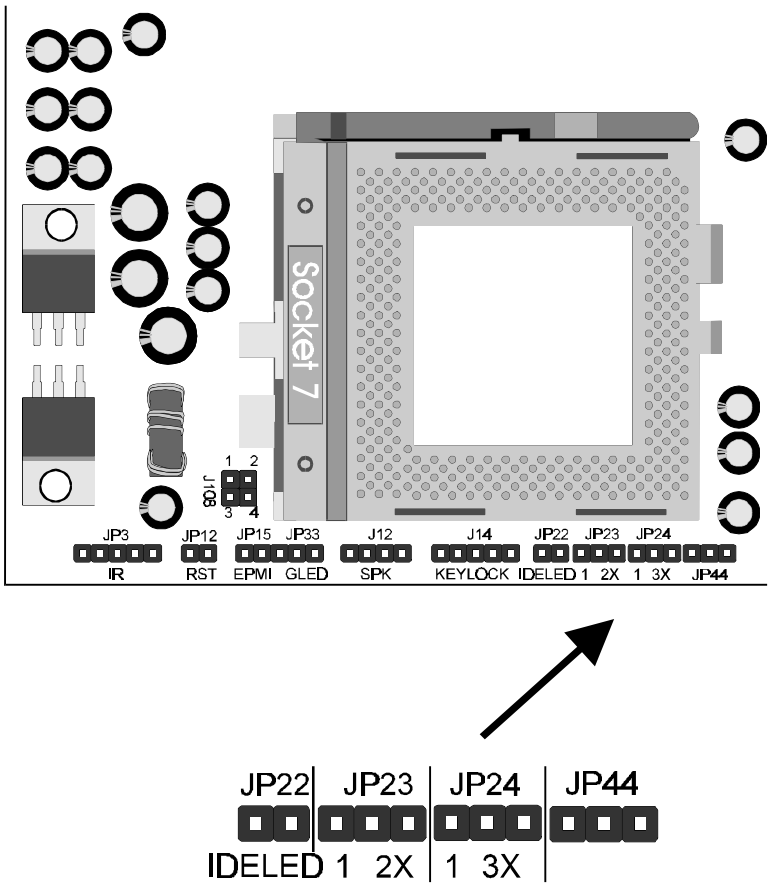
System Clock Select - JP36

	Pin 1-2	Pin 3-4	Pin 5-6
50MHz	Close	Close	Close
55MHz	Close	Open	Close
60MHz	Close	Close	Open
66MHz	Open	Close	Close

CPU Clock Speed Selection

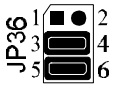
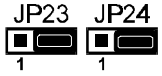
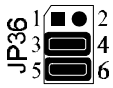
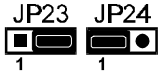
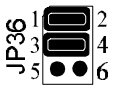
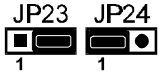
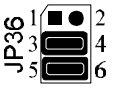
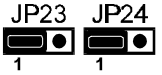
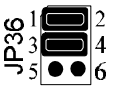
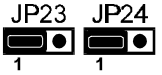
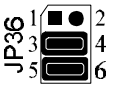
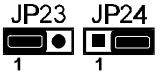
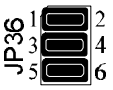
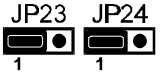
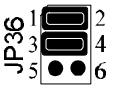
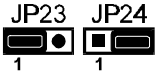
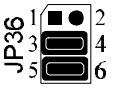
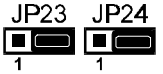
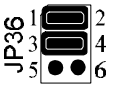
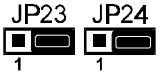
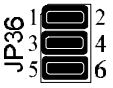
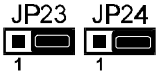
HOT-557 mainboard features a clock generator to provide adjustable system clock frequency. JP36 is a 6-pin jumper that determine the system clock frequency from 50 MHz to 66 MHz.

HOT-557 mainboard also provides Jumpers JP23 and JP24 to figure the CPU core clock multiplier. By inserting or removing jumper caps on JP23 and JP24, the user can change the **Host Bus Clock/CPU Core Clock** ratio from 1 : 1.5 to 1 : 3,5.

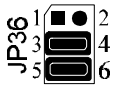
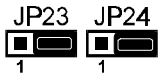
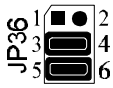
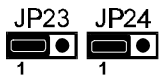
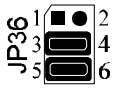
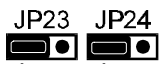
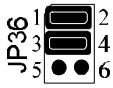
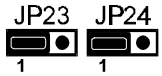
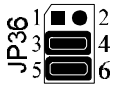
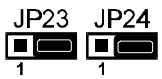
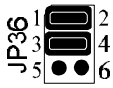
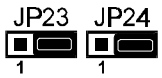
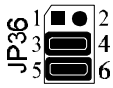
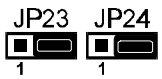
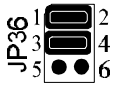
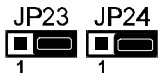
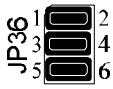
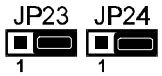


Caution:
Beware the pin sequence of Multiplier jumpers of JP23 and JP24.
Do not short pin 3 of JP23 and pin 1 of JP24 by a jumper cap.
It will cuase serve damage to the mainboard and the CPU.

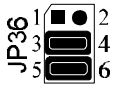
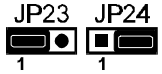
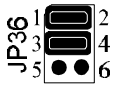
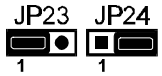
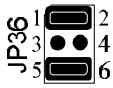
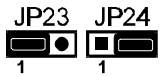
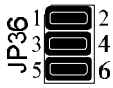
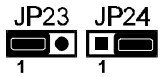
Intel Pentium Processor

CPU Type	System Clock (JP36)	Clock Multiplier (JP23, JP24)
233 MHz	66 MHz 	3,5 x 
200 MHz	66 MHz 	3 x 
180 MHz	60 MHz 	3 x 
166 MHz	66 MHz 	2,5 x 
150 MHz	60 MHz 	2,5 x 
133 MHz	66 MHz 	2 x 
125 MHz	50 MHz 	2,5 x 
120 MHz	60 MHz 	2 x 
100 MHz	66 MHz 	1,5 x 
90 MHz	60 MHz 	1,5 x 
75 MHz	50 MHz 	1,5 x 

AMD K5 / K6 Processor

CPU Type	System Clock (JP36)	Clock Multiplier (JP23, JP24)
PR2-233	66 MHz 	
PR(2)-200 (133 MHz)	66 MHz 	2 x 
PR(2)-166 (116,7 MHz)	66 MHz 	1,75 x 
PR150 (105 MHz)	60 MHz 	1,75 x 
PR133 (100 MHz)	66 MHz 	1,5 x 
PR120 (90 MHz)	60 MHz 	1,5 x 
PR100 (100 MHz)	66 MHz 	1,5 x 
PR90 (90 MHz)	60 MHz 	1,5 x 
PR75 (75 MHz)	50 MHz 	1,5 x 

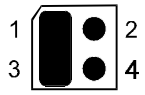
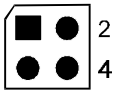
Cyrix/IBM 6x86/6x86L

CPU Type	System Clock (JP36)	Clock Multiplier (JP23, JP24)
P166+ (133 MHz)	66 MHz 	2 x 
P150+ (120 MHz)	60 MHz 	2 x 
P133+ (110 MHz)	55 MHz 	2 x 
P120+ (100 MHz)	50 MHz 	2 x 

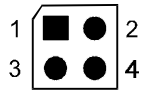
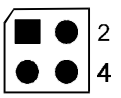
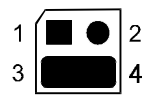
Onboard Regulator Output- J100, J101, J102, J107

HOT-557 mainboard is designed with dual onboard voltage regulator to provide single 3.3V voltage ($V_{IO}=V_{CORE}$) for Intel Pentium P54C, 3.5V for Cyrix/IBM 6x86 and AMD K5 processors, and also provide dual 3.3/2.8V voltage (V_{IO}, V_{CORE} separated) for Intel P55C (MMX), Cyrix/IBM 6x86L and AMD K6 processors.

Single Voltage Output ($V_{IO} = V_{CORE}$)

Processor	Voltage Output	J100	J108	J107	J105
Pentium P54C STD Cyrix/IBM 6x86 3.3V	3.3 V				
Pentium P54C VRE Cyrix/IBM 6x86 3.53V AMD K5 ABx	3.53 V				

Dual Voltage Output (V_{IO}, V_{CORE} separated)

Processor	Vcore Output	J100	J108	J107	J105 Vio=3.3V
Pentium P55C MMX Cyrix/IBM 6x86L	2.8 V				
AMD-K6 PR2-166/PR2-200	2.9 V				
AMD-K6 PR2-233	3.2 V				

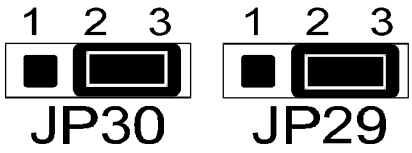
Pipeline Burst Type Cache Size Selection - JP29, JP30

HOT-557 mainboard supports 256KB or 512KB pipeline burst cache.

If the HOT-557 is ordered with no cache installed, the cache can be field upgraded by installing a **primary 256KB pipeline burst cache module** into the CELP socket.

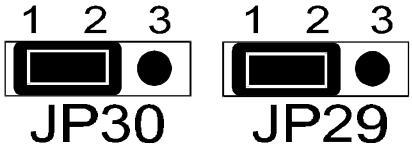
If factory option on HOT-557 mainboard integrate 256KB pipeline burst cache onboard already, the cache size can be field upgraded to 512KB by installing a **secondary 256KB pipeline burst cache module** into the CELP socket.

256KB Cache Memory



On mainboard integrate 256KB pipeline burst cache mounted, or a primary 256KB pipeline burst cache module in the CELP socket.

512KB Cache Memory



On mainboard integrate 256KB pipeline burst cache mounted and a secondary 256KB pipeline burst cache module in the CELP socket.

Note : *There are some technical difference between the primary 256KB pipeline burst cache module and secondary one, if 512KB cache memory are required, please contact your supplier for help.*

Flash EPROM Jumper - JP19

HOT-557 mainboard supports two types of flash EPROM, 5 volt and 12 volt. By setting up jumper JP19, you can update both types of flash EPROM with new system BIOS files as they come available.
JP19 Pin 2-3 Close for 5V, Pin 1-2 Close for 12V.

BIOS UPGRADES

Flash memory makes distributing BIOS upgrades easy. A new version of the BIOS can be installed from a diskette.

Please note the following when making the BIOS updates.

***** Flash utility can't work under protected/virtual mode. Memory manager like **QEMM.386**, **EMM386** should not be loaded. (or Simply bypass all **config.sys** and **autoexec.bat** on system boot up.

***** Flash utility supports both 5V and 12V Flash EEPROM.

Clear CMOS - JP21

HOT-557 mainboard supports jumper **JP21** for discharging mainboard's CMOS memory. The CMOS memory retains the system configuration information in the component of R.T.C.

You should short this jumper for a moment when you wish to clear CMOS memory, and then make sure open this jumper for normal operation to retain your new CMOS data.

Note: Clear CMOS & R.T.C function is available only when "DS12887A" or "DS12B887" is in use.

There are different ways to discharge CMOS memory between "DS12887A" and "DS12B887".

DS12887A - Turn off power, close jumper JP21 for 2 to 3 seconds then release and CMOS will be discharged.

DS12B887 - Close jumper JP21, turn on power for 2 to 3 seconds then release JP21 and turn off power, CMOS will be discharged.

Clear Password - JP9

Allows system password to be cleared by shorting jumper JP9 and turning the system on, "**Password is cleared by jumper, (JCP) !**" message will be shown on power-on screen. The system should then be turned off and the jumper JP9 should be returned to OPEN to restore normal operation. The procedure should only be done if the user password has been forgotten. (This function is not available when AMD K5 or Cyrix 6x86 CPU is in use)

Display Mode Jumper - JP7

On the HOT-557 mainboard remain jumpers JP7 for display mode selecting:

CGA40 / CGA 80:	JP7 close
Monochrome:	JP7 open
VGA:	Don't care

Factory Reserved Jumpers - JP39, JP43, JP44

On the HOT-557 mainboard remain three jumpers for future use. Normally, those jumpes were defualt by the manafacturer and need not to change by the user.

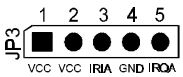
JP39 is a three pin header and default on pin 2-3 closed by a cap.
JP43 is a two pin header and default on closed by a cap.
JP44 is a three pin header and default on opened.

Connectors & Sockets

Connectors & Sockets	
ITEM	FUNCTION
J2, J3, J4, J5	On-board SIMM sockets
DIM1, DIM2	On-board 3.3V DIMM sockets
J23,J17,J18,J19	On-board PCI Slots
J20, J21, J22	On-board ISA Slots
J6	On-board PCI Primary IDE Connector
J7	On-board PCI Secondary IDE Connector
CN1	On-board Floppy Controller Connector
CN4	On-board Parallel Port Connector
CN2	On-board Serial port-1 Connector
CN3	On-board Serial Port-2 Connector
J99	On-board PS/2 Mouse Port Connector
J14	Power LED and Keylock Connector
J12	PC Speaker Connector
JP12	Hardware Reset Switch Connector
JP33	Green LED
JP15	EPMI Connector
JP22	On-board Enhanced IDE R/W LED Connector
J10, J11	Universal Serial Bus (USB) Connectors
JP3	Infra-red Communication Port Connector
JP1	Cooling Fan Connector

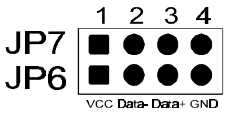
Note 1: JP3 - Infrared module connector

The main board provides a 5-pin infrared connector - JP3 as an optional infrared module for wireless transmitting and receiving. Only first 4 pins are available, left 3 pins are reserved for future use.



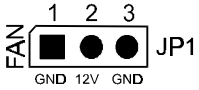
Note 2: J10, J11 - USB connectors

The main board provides two sets USB (Universal Serial Bus) connectors - J10 and J11 for USB devices use.



Note 3: JP1 - 12V cooling fan power connector

The main board provides a on-board 12V cooling fan power connector for cooling fan. Please make sure the red wire connect to +12V and black wire connect to ground (GND).



Chapter 3 Memory Configuration

The HOT-557 mainboard provides four 72-pin SIMM sockets and two 168-pin DIMM sockets that make it possible to install up to 128MB of RAM. The SIMM socket support 4MB, 8MB, 16MB, and 32MB 5V single- or double-side fast page or EDO DRAM modules, and DIMM socket support 8MB, 16MB, . . ., 3.3V single- or double-side SDRAM, fast page, or EDO modules.

Caution : The user should not populate both 5V SIMM modules & 3.3V DIMM modules at the same time.

The four SIMM sockets are arranged in two banks of two sockets each, the two DIMM socket are also arranged in two banks of one socket each. Each bank provides a 64/72-bit wide data path.

Both SIMMs in a bank must be of the same memory size and type, although the different types of memory may differ between banks. It is possible to have 70 ns fast page DRAM in one bank and 60 ns EDO DRAM in the other.

The memory configuration tables on next two pages liste the SIMMs and DIMMs memory configuration.

Table 3-1. Memory Configuration Table

SIM 1	SIM 2	SIM 3	SIM 4	DIM 1	DIM 2	TOTAL
4 MB	4 MB	——	——	——	——	8 MB
——	——	4 MB	4 MB	——	——	8 MB
4 MB	4 MB	4 MB	4 MB	——	——	16 MB
8 MB	8 MB	——	——	——	——	16 MB
——	——	8 MB	8 MB	——	——	16 MB
4 MB	4 MB	8 MB	8 MB	——	——	24 MB
8 MB	8 MB	4 MB	4 MB	——	——	24 MB
8 MB	8 MB	8 MB	8 MB	——	——	32 MB
16 MB	16 MB	——	——	——	——	32 MB
——	——	16 MB	16 MB	——	——	32 MB
4 MB	4 MB	16 MB	16 MB	——	——	40 MB
16 MB	16 MB	4 MB	4 MB	——	——	40 MB
8 MB	8 MB	16 MB	16 MB	——	——	48 MB
16 MB	16 MB	8 MB	8 MB	——	——	48 MB
16 MB	16 MB	16 MB	16 MB	——	——	64 MB
32 MB	32 MB	——	——	——	——	64 MB
——	——	32 MB	32 MB	——	——	64 MB
4 MB	4 MB	32 MB	32 MB	——	——	72 MB
32 MB	32 MB	4 MB	4 MB	——	——	72 MB
8 MB	8 MB	32 MB	32 MB	——	——	80 MB
32 MB	32 MB	8 MB	8 MB	——	——	80 MB
16 MB	16 MB	32 MB	32 MB	——	——	96 MB
32 MB	32 MB	16 MB	16 MB	——	——	96 MB
32 MB	32 MB	32 MB	32 MB	——	——	128 MB
——	——	——	——	8 MB	——	8 MB
——	——	——	——	8 MB	8 MB	16 MB
——	——	——	——	16 MB	——	16 MB
——	——	——	——	8 MB	16 MB	24 MB
——	——	——	——	16 MB	16 MB	32 MB
——	——	——	——	32 MB	——	32 MB
——	——	——	——	8 MB	32 MB	40 MB
——	——	——	——	16 MB	32 MB	48 MB
——	——	——	——	32 MB	32 MB	64 MB

Chapter 4 Award BIOS Setup

HOT-557 BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed RAM so that it retains the Setup information when the power is turned off.

Entering Setup

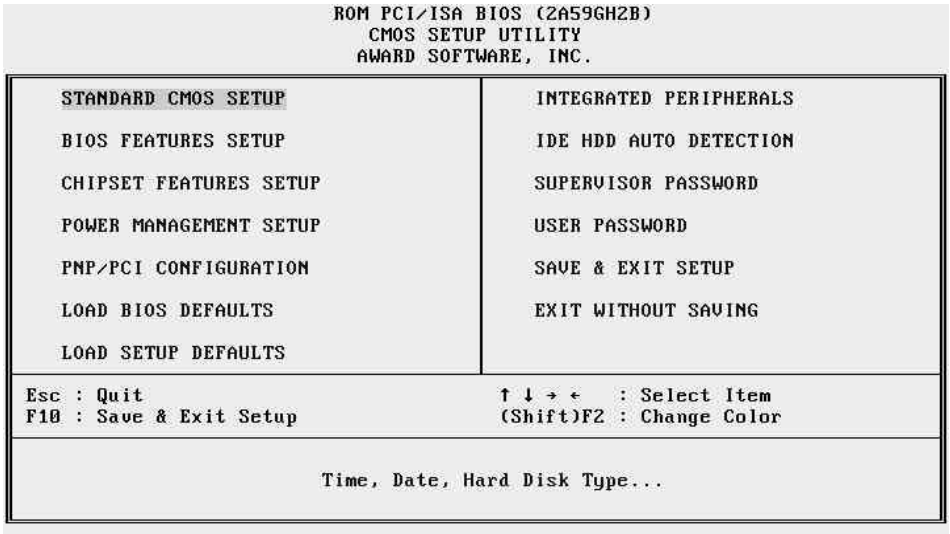
Power on the computer and press <Del> immediately will allow you to enter Setup. The other way to enter Setup is to power on the computer, when the below message appear briefly at the bottom of the screen during the POST (Power On Self Test), press <Del> key or simultaneously press <Ctrl>,<Alt>, and <Esc> keys.

TO ENTER SETUP BEFORE BOOT PRESS CTRL-ALT-ESC OR DEL KEY

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF the ON or pressing the "RESET" button on the system case. You may also restart by simultaneously press <Ctrl>,<Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to,

PRESS F1 TO CONTINUE, CTRL-ALT-ESC OR DEL TO ENTER SETUP

The Main Menu



Standard CMOS setup

This setup page includes all the items in a standard compatible BIOS.

BIOS features setup

This setup page includes all the items of Award special enhanced features.

Chipset features setup

This setup page includes all the items of chipset features.

Power Management Setup

This setup page includes all the items of Power Management features.

PCI Configuration setup

This item specifies the value (in units of PCI bus blocks) of the latency timer for the PCI bus master and the IRQ level for PCI device. Power-on with BIOS defaults

Load BIOS Defaults

BIOS defaults loads the values required by the system for the maximum performance. However, you may change the parameter through each Setup Menu.

Load Setup Defaults

Setup defaults loads the values required by the system for the O.K. performance. However, you may change the parameter through each Setup Menu.

Integrated Peripherals

This setup page includes all the items of peripheral features.

IDE HDD auto detection

Automatically configure IDE hard disk drive parameters.

Supervisor Password

Change, set, or disable supervisor password. It allows you to limit access to the system and Setup, or just to Setup.

User Password

Change, set, or disable user password. It allows you to limit access to the system and Setup, or just to Setup.

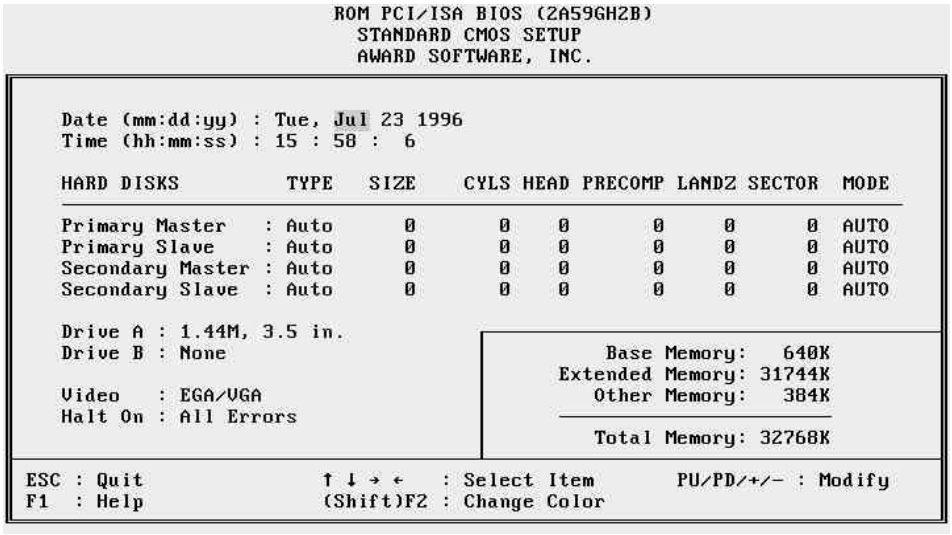
Save & Exit setup

Save CMOS value change to CMOS and exit setup

Exit without saving

Abandon all CMOS value changes and exit setup.

Standard CMOS Setup



Date

The date format is <day>, <month> <date> <year>. Press <F3> to show the calendar.

Time

The time format is <hour> <minute> <second>. The time is calculated base on the 24-hour military-time clock. For example. 5 p.m. is 17:00:00.

Drive C type/Drive D type

This item identify the types of hard disk drive C and drive D that has been installed in the computer. There are 46 predefined types and a user definable type.

Press PgUp or PgDn to select a numbered hard disk type or type the number and press <Enter>. Note that the specifications of your drive must match with the drive table. The hard disk will not work properly if you enter improper information for this item. If your hard disk drive type is not matched or listed, you can use Type User to define your own drive type manually.

If you select Type User, related information is asked to be entered to the following items. Enter the information directly from the keyboard and press <Enter>. Those information should be provided in the documentation from your hard disk vendor or the system manufacturer.

The user may also set those items to AUTO to auto configure hard disk drives parameter when system power-on.

If a hard disk drive has not been installed select NONE and press <Enter>.

Drive A type/Drive B type

This item specifies the types of floppy disk drive A or drive B that has been installed in the system.

Video

This item selects the type of adapter used for the primary system monitor that must matches your video display card and monitor. Although secondary monitors are supported, you do not have to select the type in Setup.

Error halt

This item determines if the system will stop, when an error is detected during power up.

Memory

This item is display-only. It is automatically detected by POST (Power On Self Test) of the BIOS.

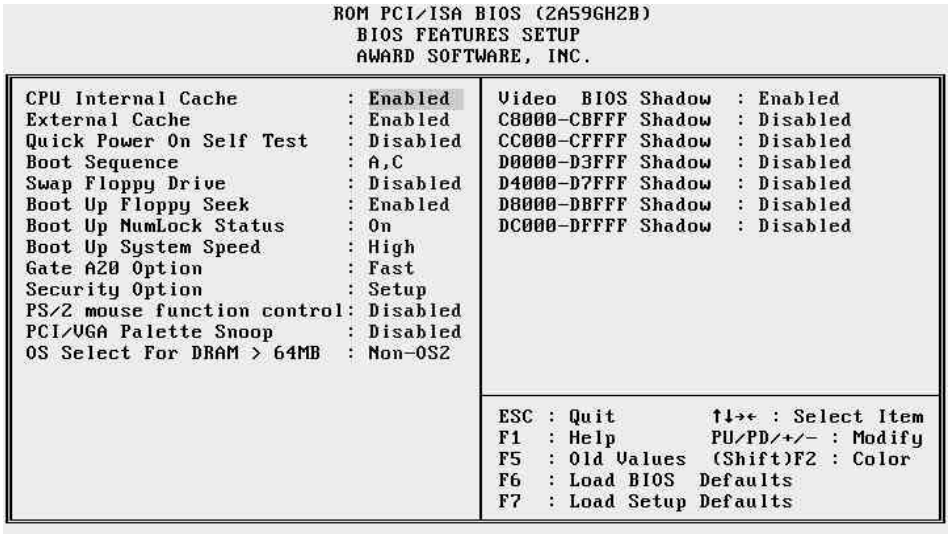
Base Memory

The POST of the BIOS will determine the amount of base (or conventional) memory installed in the system. The value of the base memory is typically 512K for systems with 512K memory installed on the mainboard, or 640K for systems with 640K or more memory installed on the mainboard.

Extended Memory

The BIOS determines how much extended memory is present during the POST. This is the amount of memory located above 1MB in the CPU's memory address map.

BIOS Features Setup



CPU Internal Cache

This item enables CPU internal cache to speed up memory access.

External Cache

This item enables the external cache to speed up memory access.

Quick Power On Self Test

This item speeds up Power On Self Test (POST) after you power on the computer. If it is set to Enabled, BIOS will shorten or skip some check items during POST.

Boot Sequence

This item determines which drive computer searches first for the disk operating system. Default value is A, C.

Swap Floppy Drive

When this item enables, the BIOS will swap floppy drive assignments so that Drive A: will function as Drive B: and Drive B: as Drive A:.

Boot Up Floppy Seek

During POST, BIOS will determine if the floppy disk drive installed is 40 or 80 tracks.

Boot Up NumLock Status

When this option enables, BIOS turns on ***Num Lock*** when system is powered on so the end user can use the arrow keys on both the numeric keypad and the keyboard.

Boot Up System Speed

This option sets the speed of the CPU at system boot time. The settings are ***High*** or ***Low***.

Gate A20 Option

When this item sets to Normal, the A20 signal is controlled by keyboard controller. When this item sets to Fast, the A20 signal is controlled by post 92 or chipset specific method.

Security Option

This item allows you to limit access to the system and Setup, or just to Setup. When ***System*** is selected, the system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.
When ***Setup*** is selected, the system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

PS/2 Mouse Control Function

This item to set the PS/2 mouse be used or not. If there a PS/2 mouse attached to your system, this item must be enabled, if not, please disabled this item to release IRQ12 for PCI device.

PCI VGA Palette Snoop

This item must be set to enabled if there is a MPEG ISA card installed in the system, and disabled if there is no MPEG ISA card installed in the system.

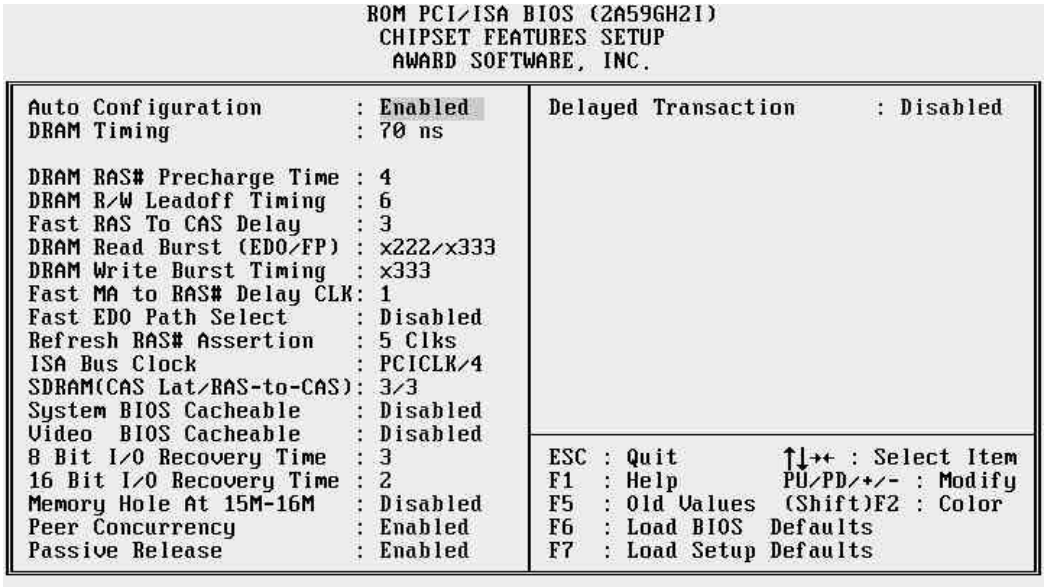
OS Select For DRAM > 64MB

This item allows you to access the memory that over 64 MB in OS/2.

Video BIOS Shadow/XXXXX-XXXXX Shadow

These items determine whether Video BIOS or optional ROM will be copied to RAM.

Chipset Features Setup



Auto Configuration

This item auto configure the following items: DRAM RAS# Precharge time, DRAM R/W Leadoff Timing, Fast RAS to CAS Delay, DRAM Read Burst, DRAM Write Burst Timing, Fast MA to RAS# Delay CLK, Fast EDO Path Select, Refresh RAS# Assertion, and ISA Bus Clock by different system clock.

DRAM Timing

This item set the DRAM Read/Write timings that the system uses. When item of "Auto Configuration" is disabled, this item will not show up.

DRAM RAS# Precharge Time

DRAM must continually be refreshed or it will lose its data. Normally, DRAM is refreshed entirely as the result of a single request. This option allows you to determine the number of CPU clocks allocated for Row Address Strobe to accumulate its charge before the DRAM is refreshed. If insufficient time is allowed, refresh may be incomplete and data lost.

This item sets the DRAM RAS Precharge Timing. The options are ***4*** and ***3*** CLKs.

DRAM R/W Leadoff Timing

This item sets the number of CPU clocks allowed before reads and writes to DRAM are performed.

7/6 : Seven clocks leadoff for reads and six clocks leadoff for writes.
6/5 : Six clocks leadoff for reads and five clocks leadoff for writes.

Fast RAS To CAS Delay

When DRAM is refreshed, both rows and columns are address separately. This setup item allows you to determine the timing of the transition from Row Address Strobe (RAS) to Column Address Strobe (CAS). The options are ***3*** and ***2*** CLKs.

DRAM Read Burst (EDO/FP)

This item set the EDO/FP DRAM Read Burst Timing. The timing used depends on the type of DRAM (EDO burst mode or standard fast page mode) on a per-bank basis. The options are ***x222/x333***, ***x333/x444***, and ***x444/x444***.

DRAM Write Burst Timing

This item set the DRAM Write Burst Timing. The timing used depends on the type of DRAM (standard page mode or EDO burst mode) on a per-bank basis. The options are ***x4444***, ***x3333***, and ***x2222***.

Fast MA to RAS# Delay CLK

This item is used to set Fast MA (Memory Address) to RAS# Delay which control DRAM Row Miss timings

Fast EDO Path Select

This item is used to defined fast path is selected for CPU to DRAM read cycles for the leadoff, the options are " ***Enable***" or "***Disable***".

Refresh RAS# Assertion

This item is used to set the number of clocks RAS# is asserted for Refresh cycles.

SDRAM (CAS Lat/RAS-to-CAS)

This item is used to set CAS# Latency and RAS# to CAS# clock for SDRAM. If SDRAMs absent, this item will not show up.

ISA Clock

This item allows the user to set ISA clock that divide from PCI clock by 3 or by 4. For example, if 166MHz Pentium processor is used, PCI clock will be 33MHz, ISA Clock will be 8.25MHz when PCI clock divided by 4, and 11MHz when PCI clock divided by 3.

System BIOS Cacheable

This item allows the user to set whether the system BIOS F000~FFFF areas are cacheable or non-cacheable.

Video BIOS Cacheable

This item allows the user to set whether the video BIOS C000~C7FF areas are cacheable or non-cacheable.

8 Bit I/O Recovery Time

The recovery time is the length of time, measured in CPU clocks, which the system will delay after the completion of an input/output request. This delay takes place because the CPU is operating so much after than the input/output bus that the CPU must be delayed to allow for the completion of the I/O.

This item allows you to determine the recovery time allowed for 8 bit I/O. Choices are from NA, 1 to 8 CPU clocks.

16-Bit I/O Recovery Time

This item allows you to determine the recovery time allowed for 16 bit I/O. Choices are from NA, 1 to 4 CPU clocks.

Memory Hole At 15M-16M

In order to improve performance, certain space in memory can be reserved for ISA cards. This memory must be mapped into the memory space below 16 MB.

Peer Concurrency

Peer concurrency means that more than one PCI device can be active at a time. Enabled this item allows multiple PCI devices can be active.

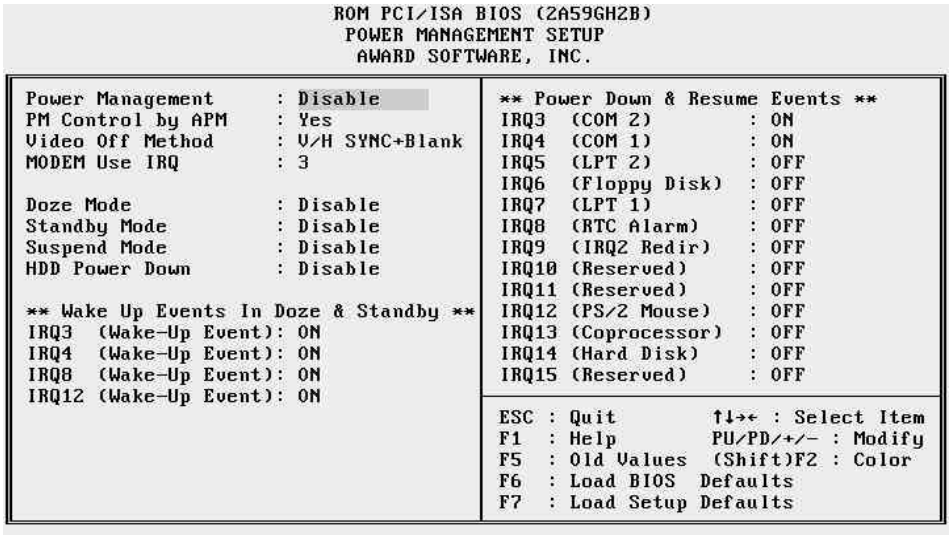
Passive Release

When enabled, the chipset provides a programmable passive release mechanism to meet the required ISA master latencies.

Delayed Transaction

Since the 2.1 revision of the PCI specification requires much tighter controls on target and master latency. PCI cycles to or from ISA typically take longer. When enabled, the chipset provides a programmable delayed completion mechanism to meet the required target latencies.

Power Management Setup



Power Management

This item determines the options of the power management function. Default value is Disable. The following pages tell you the options of each item & describe the meanings of each options.

Disabled	Global Power Management will be disabled.	**User**
Define	Users can configure their own power management.	**Min**
Saving	Predefined timer values are used such that all timers are in their maximum value.	**Max**
Saving	Predefined timer values are used such that all timers minimum value.	

PM Control by APM

If this item set to No, system BIOS will ignore and APM calls when the power is managed the system. If this item setup to Yes, system BIOS will wait for APM's prompt before it enter any PM mode e.g. ***DOZE***, ***STANDBY*** or ***SUSPEND***.

Video Off Method

Blank Screen	The system BIOS will only blanks off the screen when disabling video.	**V/H SYN**
+Blank	In addition to Blank Screen, BIOS will also turn off the V-SYNC & H-SYNC signals from VGA cards to monitor.	**DPMS**

This function is enabled for only the VGA card supporting DPM.

Doze Mode

1 Min~1 Hr Defines the continuous idle time before the system enters DOZE mode. **Disable**
System will never enter DOZE mode.

Standby Mode

1 Min~1 Hr Defines the continues idle time before the system enters STANDBY mode. **Disable** System will never enter STANDBY mode.

Suspend Mode

1 Min~1 Hr Defines the continuous idle time before the system enters SUSPEND mode. **Disable** System will never enter SUSPEND mode.

HDD Power Down

1~15Min Defines the continuous HDD idle time before the HDD enters power saving mode (motor off). **Suspend**
BIOS will turn the HDD's motor off when system is in SUSPEND mode. **Disable** HDD's motor will not be turn off.

IRQ3, 5, 8, 12 **Wake-Up Events In Doze & Standby**

If these items set to Off, the IRQ3, 5, 8 or 12 event's activity will not reactivates the system from Doze and Standby mode.

If these items set to On, the IRQ3, 5, 8 or 12 event's activity will reactivate system from Doze and Standby mode.

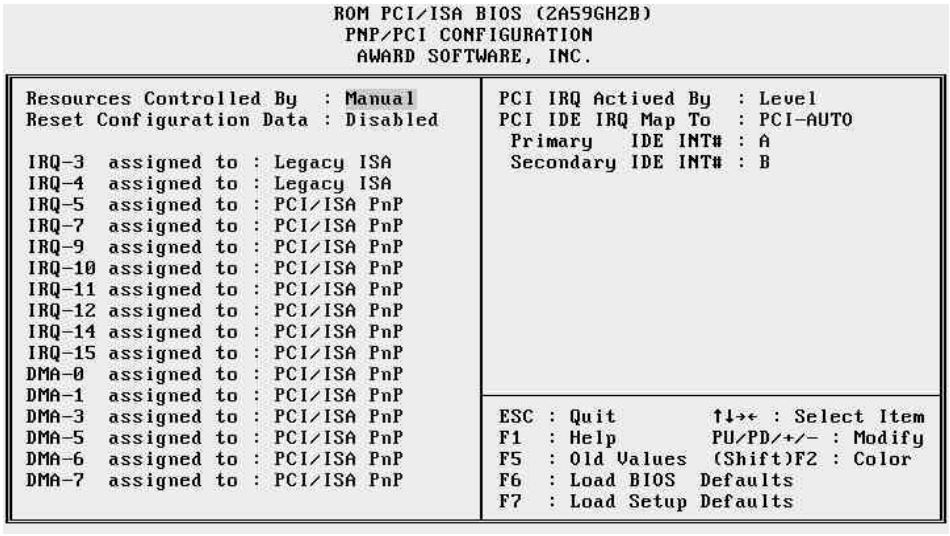
*Power Down & Resume Events **

If this items sets to Off, the event's activity will not be monitored to entering power management.

If this items sets to On, the event's activity will be monitored to entering power management.

COM Post Accessed LPT Ports Accessed Drive Ports Accessed IRQ 3 (COM 2) IRQ 4 (COM1) IRQ 5 (LPT 2) IRQ 6 (Floppy Disk) IRQ 7 (LPT 1) IRQ 8 (RTC Alarm) IRQ 9 (IRQ 2 Redir) IRQ 10 (Reserved) IRQ 11 (Reserved) IRQ 12 (PS/2 Mouse) IRQ 13(Copro-) IRQ 14 (Hard Disk) IRQ 15 (Reserved)

PCI Configuration Setup



Resources Controlled By

The Award Plug and Play BIOS has the capability to automatically configure all of the boot and Plug and Play compatible devices. However, this capability means absolutely nothing unless you are using a Plug and Play operating system as Windows 95.

Reset Configuration Data

This item allows you to determine reset the configuration data or not.

IRQ 3/4/5/7/9/10/11/12/14/15, assigned to

These items allow you to determine the IRQ assigned to the ISA bus and is not available to any PCI slot.

Choices are ***Legacy ISA*** and ***PCI/ISA PnP***.

DMA 0/1/3/5/6/7 assigned to

These items allow you to determine the DMA assigned to the ISA bus and is not available to any PCI slot.

Choices are ***Legacy ISA*** and ***PCI/ISA PnP***.

PCI IRQ Activated by

This items sets the method by which the PCI bus recognize that an IRQ service is being requested by a device. Under all circumstances, you should not change the default configuration unless advised otherwise by your system's manufacturer. Choices are ***Level***(default) and ***Edge***.

PCI IDE IRQ Map to

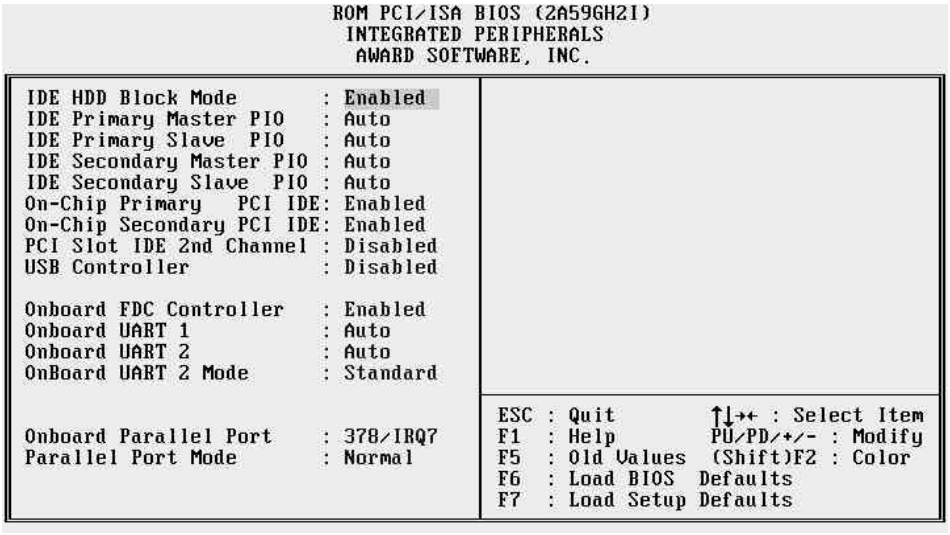
This items allows you to configure your system to the type of IDE disk controller in use. By default, Setup assumes that your controller is an ISA device rather than a PCI controller.

If you have equipped your system with a PCI controller, changing this allows you to specify which slot has the controller and which PCI interrupt (A, B, C or D) is associated with the connected hard drives.

Remember that this setting refers to the hard disk drive itself, rather than individual partitions. Since each IDE controller supports two separate hard disk drivers, you can select the INT# for each. Again, you will note that the primary has a lower interrupt than the secondary as described in " *Slot x Using INT#*" above.

Selecting "*PCI Auto*" allows the system to automatically determine how your IDE disk system is configured.

Integrated Peripherals



IDE HDD Block Mode

This item is used to set IDE HDD Block Mode. If your IDE Hard Disk supports block mode, then you can enable this function to speed up the HDD access time. If not, please disable this function to avoid HDD access error.

IDE Primary/Secondary Master PIO

In this item, there are five modes defined in manual mode and one automatic mode. There are ***0***, ***1***, ***2***, ***3***, ***4***, and ***AUTO***. The default settings for on board Primary/Secondary Master PIO timing is Auto.

IDE Primary/Secondary Slave PIO

In this item, there are five modes defined in manual mode and one automatic mode. There are ***0***, ***1***, ***2***, ***3***, ***4***, and ***AUTO***. The default settings for on board Primary/Secondary Slave PIO timing is Auto.

On-Chip Primary PCI IDE

This item is used to defined on chip Primary PCI IDE controller is " ***Enable***" or "***Disable***" setting.

On-Chip Secondary PCI IDE

This item is used to defined on chip Secondary PCI IDE controller is "***Enable***" or "***Disable***" setting.

PCI Slot IDE 2nd channel

This item is used to defined add-on PCI IDE secondary controller is "***Enable***" or "***Disable***" setting.

Onboard FDC Control

This item specifies onboard floppy disk drive controller. This setting allows you to connect your floppy disk drives to the onboard floppy connector. Choose the "Disabled" settings if you have a separate control card.

Onboard UART1/2

This item is used to define onboard serial port 1/Port2 to ***3F8/IRQ4***, ***2F8/IRQ3***, ***3E8/IRQ4***, ***2E8/IRQ3***, ***Auto*** or ***Disabled***.

Onboard UART 2 Mode

The main board support IrDA(HPSIR) and Amplitudes Shift Keyed IR(ASKIR) infrared through COM 2 port. This item specifies onboard Infra Red mode to ***HPSIR***, ***ASKIR*** or ***Standard (Disabled)***.

IR Duplex Mode

This item specifies onboard infrared transfer mode to ***full-duplex*** or ***half-duplex***.

Onboard Parallel Port

This item specifies onboard parallel port address to ***378H***, ***278H***, ***3BCH*** or ***Disabled***.

Parallel Port Mode Mode

This item specifies onboard parallel port mode. The options are ***SPP*** (Standard Parallel Port), ***EPP***(Enhanced Parallel Port), ***ECP*** (Extended Capabilities Port), and ***EPP+ECP***.

ECP Mode Use DMA

This item specifies DMA (Direct Memory Access) channel when ECP device is in use. The options are DMA ***1*** and DMA ***3.***

This item will not show up when SPP and EPP printer mode is selected

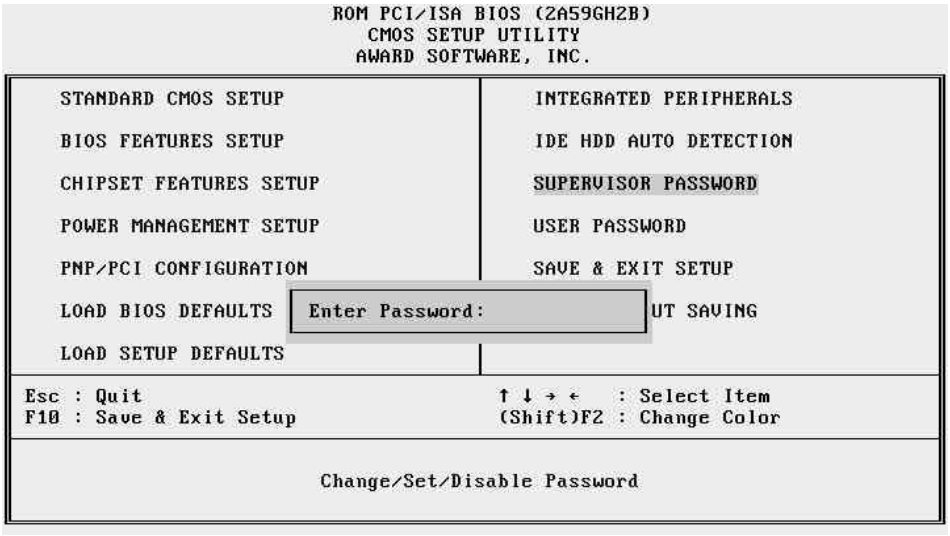
Paralle Port EPP Mode Type

This item specifies EPP type when EPP device is in use. The options are ***EPP1.7*** and ***EPP1.9.***

This item will not show up when SPP and ECP parallel mode is selected

Password Setting

This section describes the two access modes that can be set using the options found on the Supervisor Password and User Password.



Supervisor Password and User Password

The options on the Password screen menu make it possible to restrict access to the Setup program by enabling you to set passwords for two different access modes: Supervisor mode and User mode.

In general, Supervisor mode has full access to the Setup options, whereas User mode has restricted access to the options. Thus by setting separate Supervisor and User password, a system supervisor can limit who can change critical Setup values.

Enter Password

Type the password, up to eight characters, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password.

To disable password, just press <Enter> when you are prompted to enter password. A message will confirm the password being disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

Password Disable

If you select System at Security Option of BIOS Features Setup Menu, you will be prompted for the password every time the system is rebooted or any time you try to enter Setup. If you select Setup at Security Option of BIOS Features Setup Menu, you will be prompted only when you try to enter Setup.

Warning : Retain a safe record of your password. If you've forgotten or loosed the password, the only way to access the system is to clear CMOS memory, please refer to "Clear CMOS" or "Clear Password" section.