

HOT-541

Pentium processor

Based PCI MAIN BOARD

User's Manual

FCC Notice:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy. If not installed and used properly, in strict accordance with the manufacturer's instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

Reorient or relocate the receiving antenna.

Increase the separation between the equipment and receiver.

Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

Consult the dealer or an experienced radio/television technician for help and for additional suggestions.

The user may find the following booklet prepared by the Federal Communications Commission helpful "How to Identify and Resolve Radio-TV Interference Problems." This booklet is available from the U.S. Government Printing Office, Washington, DC 20402, Stock 004-000-00345-4

FCC Warning

The user is cautioned that changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

Note : In order for an installation of this product to maintain compliance with the limits for a Class B device, shielded cables and power cord must be used.

NOTICE

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Manual Ver 2.3 (For Mainboard Ver 2.5)

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Preface

HOT-541 mainboard is a highly integrated IBM PC/AT compatible system board. The design will accept Intel Pentium, Cyrix 6x86 and AMD5k86 processors and also features high-performance asynchronous and pipeline burst secondary cache memory support with size of 256KB and 512KB. The memory subsystem is designed to support up to 128 MB of EDO RAM or standard Fast Page DRAM in standard 72-pin SIMM socket. A type 7 Pentium processor socket provides access to future processor enhancements.

HOT-541 provides a new level of I/O integration. Intel's 82430 PCIset chip set provides increased integration and improved performance over other chip set designs. The 82430 PCIset chipset provides an integrated Bus Mastering IDE controller with two high performance IDE interfaces for up to four IDE devices.

The onboard Super I/O controller provides the standard PC I/O functions: floppy interface, two FIFO serial ports, an IR device port and a SPP/EPP/ECP capable parallel port.

Up to four PCI local bus slots provide a high bandwidth data path for data-movement intensive functions such as graphics, and up to four ISA slots complete the I/O function.

The HOT-541 provides the foundation for cost effective, high performance, highly expandable platforms, which deliver the latest in Pentium processor and I/O standard

Chapter 1 Introduction

Specification

CPU Function

- Pentium processor clock : 75~200MHz
- Cyrix 6x86 CPU clock : 80~133MHz
- AMD5k86 CPU clock : 66~100MHz
- Optional VRM socket for future voltage required

Chipset

- Intel PCISet 82437FX, 82438FX, and 82371FB

Memory

- 64-bit wide memory
- Supports two banks of EDO RAM and Fast Page DRAM ranging from 8MB to 128MB
- Supports 4MB, 8MB, 16MB and 32MB with or without parity 72-pins SIMMs

Cache Memory

- Integrated L2 write-back cache controller
 - Pipeline Burst or standard SRAM
 - 256KB or 512KB Direct Mapped

Power Management Function

- Provides four power management modes : Full on, Doze, Standby, and Suspend
- Supports Microsoft APM
- Provides EPMI (External Power Management Interrupt) pin

Expansions

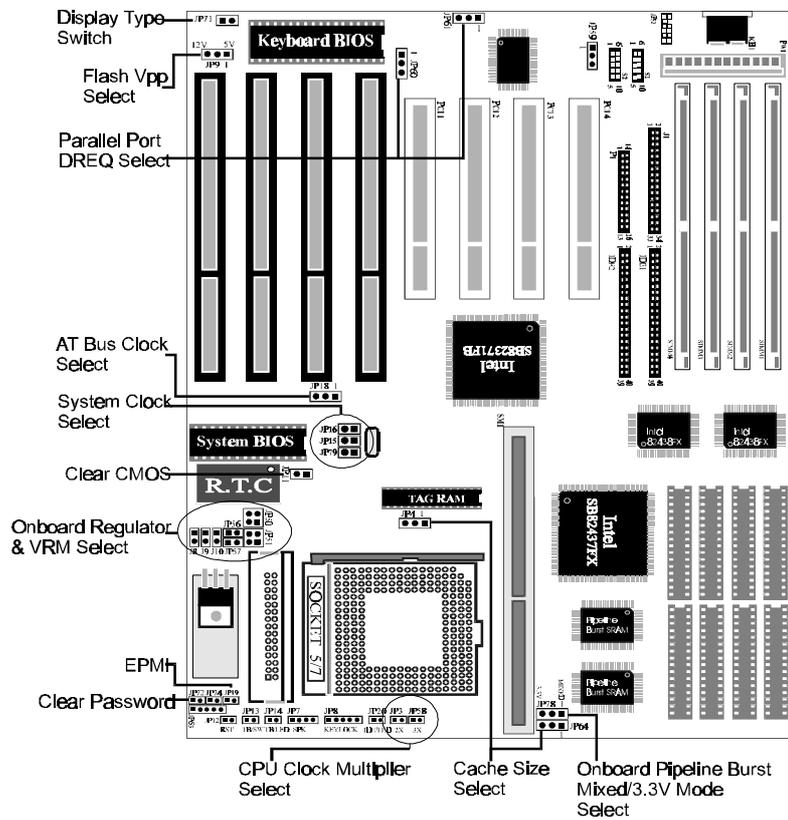
- 32-bit PCI bus slot x 4
- 16-bit ISA bus slot x 4
- 2-channel PCI IDE port
 - Support up to 4 IDE devices
 - PIO Mode 4 transfers up to 16 MB/sec
 - Integrated 8 x 32-bit buffer for PCI IDE burst transfers
- One floppy port
- One parallel port
 - Supports **SPP** (PS/2 compatible bidirectional Parallel Port), **EPP** (Extended Parallel Port), and **ECP** (Extended Capabilities Port) high performance parallel port.
- Two serial ports
 - Supports 16C550 compatible UARTS.
 - Supports serial InfraRed communication.
- One PS/2 mouse port

Board Design

- Dimension 22cm x 28cm

Chapter 2 Hardware Installation

Jumpers



CPU Clock Speed Selection

HOT-541 mainboard features a clock generator to provide adjustable system clock frequency. JP15, JP16 and JP79 are all 2-pin jumpers which determine the system clock frequency from 40MHz to 66MHz.

HOT-541 mainboard also provides JP3 and JP58 to figure up CPU core clock multiplier. By inserting or removing jumper caps on JP3 and JP58, the user can change the **Host Bus Clock /CPU Core Clock** ratio from 1 : 1.5 to 1 : 3.

Intel Pentium

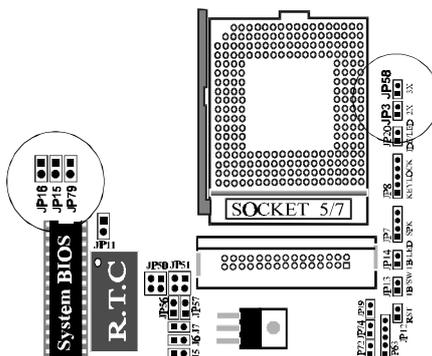
CPU Clock Speed	JP16, JP15, JP79	System Clock	JP3 & JP58	CPU Bus / Core Ratio
75 MHz Pentium Processor		50 MHz		1 : 1.5
90 MHz Pentium Processor		60 MHz		1 : 1.5
100 MHz Pentium Processor		66 MHz		1 : 1.5
120 MHz Pentium Processor		60 MHz		1 : 2
125 MHz Pentium Processor		50 MHz		1 : 2,5
133 MHz Pentium Processor		66 MHz		1 : 2
150 MHz Pentium Processor		60 MHz		1 : 2,5
150 MHz Pentium Processor		50 MHz		1 : 3
166 MHz Pentium Processor		66 MHz		1 : 2.5
180 MHz Pentium Processor		60 MHz		1 : 3
200 MHz Pentium Processor		66 MHz		1 : 3

Cyrix 6x86

CPU Clock Speed	JP16, JP15, JP79	System Clock	JP3 & JP58	CPU Bus/Core Ratio
80 MHz Cyrix 6x86-P90+		40 MHz		1 : 2
100 MHz Cyrix 6x86-P120+		50 MHz		1 : 2
120 MHz Cyrix 6x86-P150+		60 MHz		1 : 2
133 MHz Cyrix 6x86-P166+		66 MHz		1 : 2

AMD 5k86

CPU Clock Speed	JP16, JP15, JP79	System Clock	JP3 & JP58	CPU Bus/Core Ratio
66 MHz AMD5k86 - P75		66 MHz		1 : 1
75 MHz AMD5k86 - P75		50 MHz		1 : 1.5
90 MHz AMD5k86 - P90		60 MHz		1 : 1.5
100 MHz AMD5k86 - P100		66 MHz		1 : 1.5

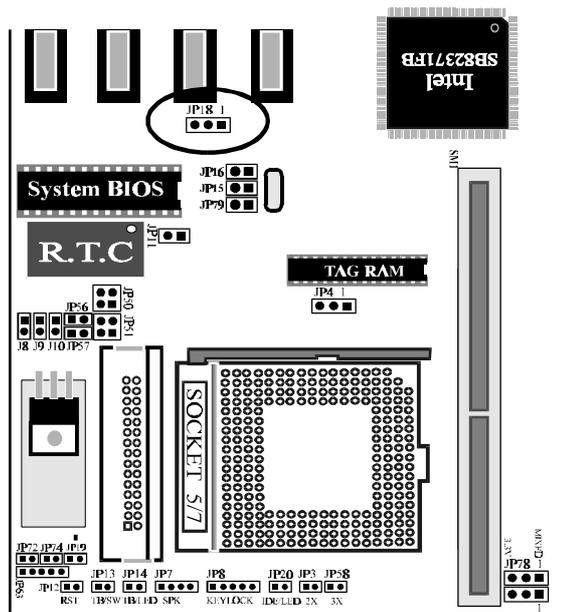


AT Bus Clock Selection - JP18

HOT-541 mainboard provides a jumper JP18 to set the AT bus (ISA bus) clock that divide from system clock, the available settings are SYSCLK/6 and SYSCLK/8.

Please refer the follow table to set the AT bus clock.

System Clock	JP18	Divided by	AT Bus Clock
40 MHz	 JP18	6	6.67 MHz
50 MHz	 JP18	6	8.33 MHz
60 MHz	 JP18	8	7.50 MHz
66 MHz	 JP18	8	8.25 MHz

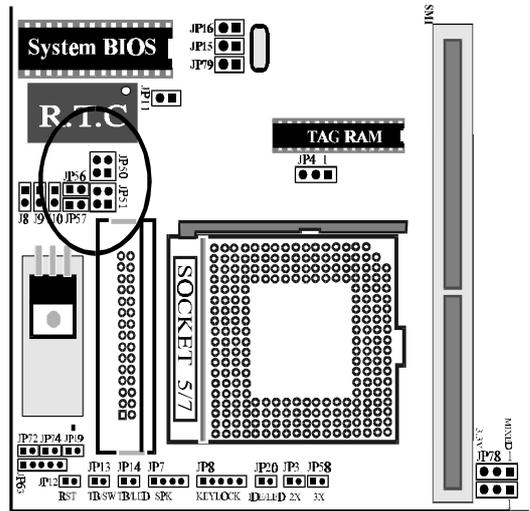


Onboard regulator & VRM Selection - JP50,51,56,57

HOT-541 mainboard is designed an onboard voltage regulator to provide 3.3V ranger for pentium, 6x86 and 5k86, and optional VRM (voltage regulator module) socket for VRM to provide 3.3/2.5V ranger for P55C processors.

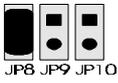
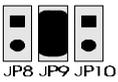
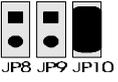
Nomarily, VRM supports both voltage level , but some particular VRM, they only provide 2.5V and require onboard regulator to complement 3.3V to P55C.

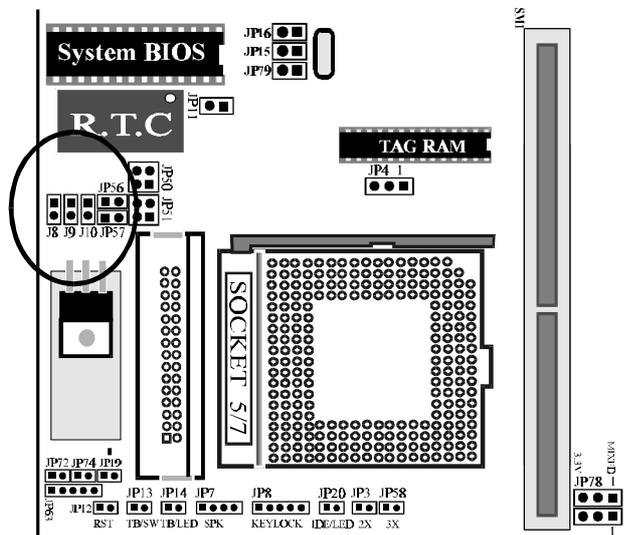
Voltage Output	JP50, 51, 56, 57	Power Supply Path
Onboard regulator for Pentium processor, Cyrix 6x86, AMD5k86 (Default)		3.3~3.6V ranger from onboard regulator
Add-on VRM for P55C		3.3V & 2.5V from add-on VRM
Onboard regulator and Add-on VRM for P55C		3.3V ranger from onboard regulator, 2.5V from add-on VRM



Onboard Voltage Regulator Output Selection - JP8,9,10

HOT-541 mainboard is designed to offer several CPU voltages level for Pentium processor, 6x86, and 5k86 family requirements. 3.3V for standard 75/90/100/120/133/166 MHz Pentium processors, 3.45V for VR s-spec Pentium processors (3.3V +5% -0%), and 3.6V for VRE s-spec Pentium processors (3.45V to 3.6V).

Voltage Output	J8, J9, J10	Processors
3.3 V±5%		Pentium Processor STD/VR Cyrrix 6x86 AMD5k86
3.45 V±5%		Pentium Processor VR/VRE Cyrrix 6x86 AMD5k86
3.6 V±5%		Pentium processor VRE



Cache Type Selection

HOT-541 mainboard support several types cache scheme including onboard standard asynchronous cache RAM, standard asynchronous cache module, onboard pipeline burst cache SRAM, and pipeline burst cache module.

Onboard standard asynchronous cache

HOT-541 mainboard provides 9 pcs DIP socket to accommodate standard asynchronous cache, with default size of 256KB and upgradable to 512KB. (please refer to section of " **Standard Type Cache Selection** ")

Onboard pipeline burst cache RAM

A factory option on HOT-541 mainboard is an integrated 256KB external cache implemented with two 32K x 32 pipeline burst SRAM devices soldered to the mainboard. A 5v 32KB x 8 external Tag SRAM is required.

Pipeline Burst cache module

If the HOT-541 is ordered with no cache installed, the cache can be added later in a field upgrade by installing a 256KB pipeline burst cache module into the CELP socket.

If factory option on HOT-541 mainboard integrate 256KB pipeline burst cache installed already, the cache size can be field upgrade to 512KB by installing a 256KB pipeline burst cache module into the CELP socket.

(please refer to section of " **Pipeline Burst Type Cache Selection** ")

Standard Type Cache Size Selection - JP4

HOT-541 mainboard supports extended standard cache memory sizes of 256KB and 512KB. Cache memory is realized by eight Data SRAM and one Tag SRAM. The 512KB configuration uses eight 64KB x 8 SRAM, each of SRAM fills the entire socket. The 256KB configuration uses eight 32KB x 8 SRAM, note that each of the 32KB x 8 SRAM do not fill the entire socket, just leaving the top four pin holes empty.

All Data SRAM must be 3.3V mode or mixed mode, and Tag SRAM must be 5V. All of Data and Tag SRAM must with a speed of 15ns or faster.

Jumper JP78 is provided for setting Data SRAM mode,

for 3.3V mode SRAM: 

and for mixed mode SRAM: 

256KB Cache Memory



Cache Size	Data RAM	Tag RAM U24
	U25, U26, U27, U28 U35, U36, U37, U38	
256KB	32K x 8	32K x 8

512KB Cache Memory



Cache Size	Data RAM	Tag RAM U24
	U25, U26, U27, U28 U35, U36, U37, U38	
512KB	64K x 8	32K x 8

Pipeline Burst Type Cache Size Selection - JP4, JP64

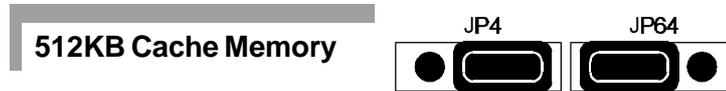
HOT-541 mainboard supports 256KB or 512KB pipeline burst cache size.

If the HOT-541 is ordered with no cache installed, the cache can be field upgraded by installing a **first 256KB pipeline burst cache module** into the CELP socket.

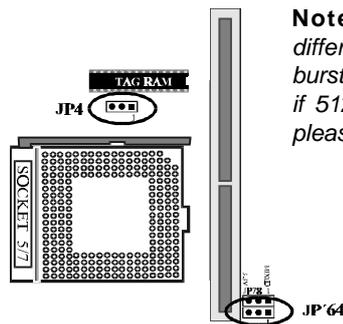
If factory option on HOT-541 mainboard integrate 256KB pipeline burst cache onboard mounted already, the cache size can be field upgraded to 512KB by installing a **secondary 256KB pipeline burst cache module** into the CELP socket.



On mainboard integrate 256KB pipeline burst cache mounted, or a first 256KB pipeline burst cache module in the CELP socket.



On mainboard integrate 256KB pipeline burst cache mounted and a secondary 256KB pipeline burst cache module in the CELP socket.



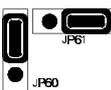
Note : *There are some technical difference between first 256KB pipeline burst cache module and secondary one, if 512KB cache memory are required, please contact your supplier for help .*

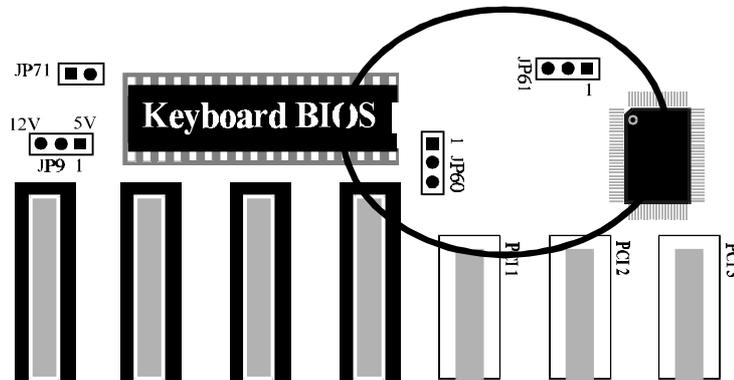
Parallel Port DREQ Selection - JP60, JP61

HOT-541 mainboard onboard parallel port supports ECP mode (Extended Capabilities Port), and provide two available DMA Request lines DREQ1 and DREQ3 for it.

When an ECP mode device is in use, the user may assign DREQ1 or DREQ3 for parallel port. If SPP/EPP mode is selected, the user may ignore those jumpers.

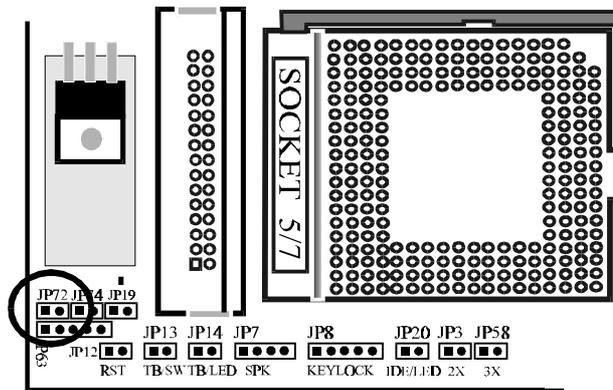
Jumper JP59 factory default on 

Parallel Port DMA Selection	JP60, JP61
Parallel Port ECP Mode DMA Request 1 (default)	
Parallel Port ECP Mode DMA Request 3	



Clear Password - JP72

Allows system password to be cleared by shorting jumper JP72 and turning the system on, "Password is cleared by jumper, (JCP)!" message will show up on power-on screen. The system should then be turned off and the jumper JP72 should be returned to OPEN to restore normal operation. The procedure should only be done if the user password has been forgotten. (This function may not be available when Cyrix 6x86 CPU is in use)



Flash EPROM Jumper - JP9

HOT-541 mainboard supports two types of flash EPROM, 5 volt and 12 volt. By setting up jumper JP9, you can update both types of flash EPROM with new system BIOS files as they come available.
JP9 open for 5V, Pin 2-3 close for 12V.

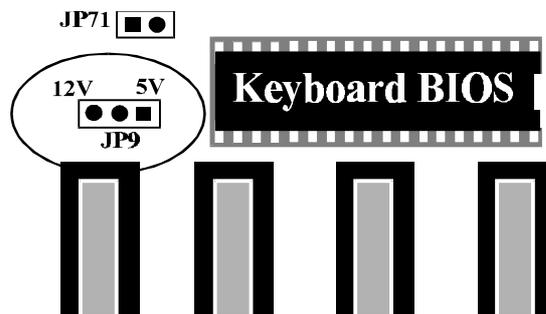
BIOSUPGRADES

Flash memory makes distributing BIOS upgrades easy. A new version of the BIOS can be installed from a diskette.

The flash upgrade utility, **Awdflash.exe**, has two notice for BIOS upgrades:

Flash utility can't work under protected/virtual mode. Memory manager like **QEMM.386**, **EMM386** should not be loaded. (or simply bypass all **config.sys** and **autoexec.bat** on system boot up.

Flash utility supports both 5V and 12V Flash EEPROM.



Clear CMOS - JP11

HOT-541 mainboard supports jumper **JP11** for discharge mainboard's CMOS memory. The CMOS memory retains the system configuration information in the component of R.T.C.

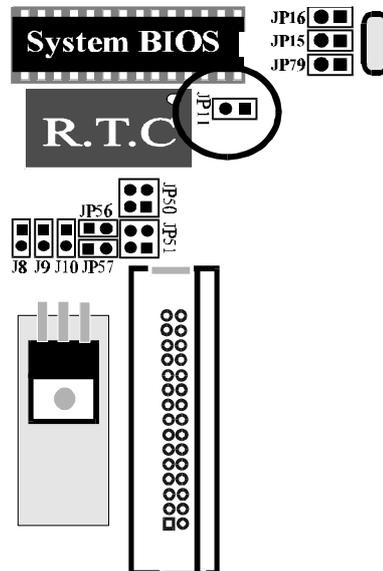
You should short this jumper for a moment when you wish to clear CMOS memory, and then make sure open this jumper for normal operation to retain your new CMOS data.

Note: Clear CMOS & R.T.C function available only when "DS12887A" or "DS12B887" are in use.

There are different ways to discharge CMOS memory between "DS12887A" and "DS12B887".

DS12887A - Turn off power, close jumper JP11 for 2 to 3 seconds then release and CMOS will be discharged.

DS12B887 - Close jumper JP11, turn on power during 2 to 3 seconds then release JP11 and turn off power, CMOS will be discharged.

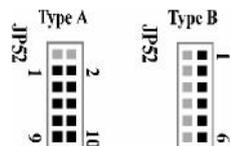


Connectors

Connectors	
ITEM	FUNCTION
IDE1	On-board PCI Primary IDE Connector
IDE2	On-board PCI Secondary IDE Connector
J1	On-board Floppy Controller Connector
P1	On-board Parallel Port Connector
S1	On-board Serial port-1 Connector
S2	On-board Serial Port-2 Connector
JP52	On-board PS/2 Mouse Port Connector
JP8	Power LED and Keylock Connector
JP7	PC Speaker Connector
JP12	Hardware Reset Switch Connector
JP14	Turbo LED Connector
JP74	Green LED
JP19	EPMI Connector
JP20	On-board Enhanced IDE R/W LED Connector
JP71	Display type (Color/Mono) Switcher

PS/2 Mouse Connector

HOT-541 mainboard provides two type of PS/2 style mouse connectors, type A and type B, the right table shows the pinout connection for each type.



PIN	TYPE A	TYPE B
1	Empty	Clock
2	Ground	Empty
3	Clock	Ground
4	Ground	VCC
5	VCC	Data
6	Empty	Empty
7	Empty	
8	Empty	
9	Data	
10	Empty	

Chapter 3 Memory Configuration

HOT-541 mainboard support great flexibility of different on-board fast page mode and EDO mode memory up to 128MB.

On-board four SIMM sockets are organized into two banks, with two SIMM sockets assigned to one memory bank. HOT-541 mainboard supports 4MB, 8MB, 16MB and 32MB single-side or double-side 72-pin SIMMs.

The table on next page shows the possible memory combinations of HOT-541 mainboard.

Notes: *Fast page mode SIMM and EDO SIMM can not mixed within the same memory bank.*

HOT-541 Memory Configuration Reference Table		
SIMM 1, 2	SIMM 3, 4	TOTAL
4 MB	Empty	8 MB
8 MB	Empty	16 MB
16 MB	Empty	32 MB
32 MB	Empty	64 MB
Empty	4 MB	8 MB
Empty	8 MB	16 MB
Empty	16 MB	32 MB
Empty	32 MB	64 MB
4 MB	4 MB	16 MB
4 MB	8 MB	24 MB
4 MB	16 MB	40 MB
4 MB	32 MB	72 MB
8 MB	4 MB	24 MB
8 MB	8 MB	32 MB
8 MB	16 MB	48 MB
8 MB	32 MB	80 MB
16 MB	4 MB	40 MB
16 MB	8 MB	48 MB
16 MB	16 MB	64 MB
16 MB	32 MB	96 MB
32 MB	4 MB	72 MB
32 MB	8 MB	80 MB
32 MB	16 MB	96 MB
32 MB	32 MB	128 MB

Chapter **4** Award BIOS Setup

HOT-541's BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed RAM so that it retains the Setup information when the power is turned off.

Entering Setup

Power on the computer and press immediately will allow you to enter Setup. The other way to enter Setup is to power on the computer, when the below message appear briefly at the bottom of the screen during the POST (Power On Self Test), press key or simultaneously press <Ctrl>,<Alt>, and <Esc> keys.

TO ENTER SETUP BEFORE BOOT PRESS CTRL-ALT-ESC OR DEL KEY

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF the ON or pressing the "RESET" button on the system case. You may also restart by simultaneously press <Ctrl>,<Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to,

PRESS F1 TO CONTINUE, CTRL-ALT-ESC OR DEL TO ENTER SETUP

The Main Menu

ROM PCI/ISA BIOS (2A59CH2E)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC.

STANDARD CMOS SETUP	IDE HDD AUTO DETECTION
BIOS FEATURES SETUP	PASSWORD SETTING
CHIPSET FEATURES SETUP	SAVE & EXIT SETUP
POWER MANAGEMENT SETUP	EXIT WITHOUT SAVING
PCI CONFIGURATION SETUP	
LOAD BIOS DEFAULTS	
LOAD SETUP DEFAULTS	
Esc : Quit	↑ ↓ → ← : Select Item
F10 : Save & Exit Setup	(Shift)F2 : Change Color
Time, Date, Hard Disk Type...	

Standard CMOS setup

This setup page includes all the items in a standard compatible BIOS.

BIOS features setup

This setup page includes all the items of Award special enhanced features.

Chipset features setup

This setup page includes all the items of chipset features.

Power Management Setup

This setup page includes all the items of Power Management features.

PCI Configuration setup

This category specifies the value (in units of PCI bus blocks) of the latency timer for this PCI bus master and the IRQ level for PCI device. Power-on with BIOS defaults

Load BIOS Defaults

BIOS defaults loads the values required by the system for the maximum performance. However, you may change the parameter through the Option Setup Menu.

Load Setup Defaults

Setup defaults loads the values required by the system for the minimum performance. However, you may change the parameter through the Setup Menu.

IDE HDD auto detection

Automatically configure IDE hard disk drive parameters.

Password setting

Change, set, or disable password. It allows you to limit access to the system and Setup, or just to Setup.

Save & Exit setup

Save CMOS value change to CMOS and exit setup

Exit without saving

Abandon all CMOS value changes and exit setup.

Standard CMOS Setup

BOM PCI/ISA BIOS (2A59CH2A)
STANDARD CMOS SETUP
AWARD SOFTWARE, INC.

Date (mm:dd:yy) : Sat, Aug 12 1995									
Time (hh:mm:ss) : 17 : 18 : 33									
HARD DISKS	TYPE	SIZE	CYLS	HEAD	PRECOMP	LANDZ	SECTOR	MODE	
Primary Master	: Auto	0	0	0	0	0	0	AUTO	
Primary Slave	: Auto	0	0	0	0	0	0	AUTO	
Secondary Master	: Auto	0	0	0	0	0	0	AUTO	
Secondary Slave	: Auto	0	0	0	0	0	0	AUTO	
Drive A : 1.44M, 3.5 in.								Base Memory: 640K	
Drive B : None								Extended Memory: 15360K	
Video : EGA/UGA								Other Memory: 384K	
Halt On : All Errors								Total Memory: 16384K	
ESC : Quit		↑ ↓ → ← : Select Item		PU/PD/+/- : Modify					
F1 : Help		(Shift)F2 : Change Color							

Date

The date format is <day>, <date> <month> <year>. Press <F3> to show the calendar.

Time

The time format is <hour> <minute> <second>. The time is calculated based on the 24-hour military-time clock. For example, 5 p.m. is 17:00:00.

Daylight saving

The category adds one hour to the clock when daylight-saving time begins. It also subtracts one hour when standard time begins.

Drive C type/Drive D type

The category identifies the types of hard disk drive C or drive D that has been installed in the computer. There are 46 predefined types and a user-definable type. Type 1 to Type 46 are predefined. Type User is user-definable.

Press PgUp or PgDn to select a numbered hard disk type or type the number and press <Enter>. Note that the specifications of your drive must match with the drive table. The hard disk will not work properly if you enter improper information for this category. If your hard disk drive type is not matched or listed, you can use Type User to define your own drive type manually.

If you select Type User, related information is asked to be entered to the following items. Enter the information directly from the keyboard and press <Enter>. Those information should be provided in the documentation from your hard disk vendor or the system manufacturer.

If a hard disk drive has not been installed select NONE and press <Enter>.

Drive A type/Drive B type

The category identify the types of floppy disk drive A or drive B that has been installed in the computer.

Video

The category selects the type of adapter used for the primary system monitor that must matches your video display card and monitor. Although secondary monitors are supported, you do not have to select the type in Setup.

Error halt

The category determines whether the computer will stop off an error is detected during power up.

Memory

The category is display-only which is determined by POST (Power On Self Test) of the BIOS.

Base Memory

The POST of the BIOS will determine the amount of base (or conventional) memory installed in the system. The value of the base memory is typically 512K for systems with 512K memory installed on the mainboard, or 640K for systems with 640K or more memory installed on the mainboard.

Extended Memory

The BIOS determines how much extended memory is present during the POST. This is the amount of memory located above 1MB in the CPU's memory address map.

BIOS Features Setup

ROM PCI/ISA BIOS (2A59CH2C) BIOS FEATURES SETUP AWARD SOFTWARE, INC.			
CPU Internal Cache	: Enabled	Video BIOS Shadow	: Enabled
External Cache	: Enabled	C8000-CBFFF Shadow	: Disabled
Quick Power On Self Test	: Disabled	CC000-CFFFF Shadow	: Disabled
Boot Sequence	: A, C	D0000-D3FFF Shadow	: Disabled
Swap Floppy Drive	: Disabled	D4000-D7FFF Shadow	: Disabled
Boot Up Floppy Seek	: Enabled	D8000-DBFFF Shadow	: Disabled
Boot Up NumLock Status	: On	DC000-DFFFF Shadow	: Disabled
Boot Up System Speed	: High		
Gate A20 Option	: Fast		
Security Option	: Setup		
PS/2 mouse function control	: Enabled		
PCI/UGA Palette Snoop	: Disabled		
OS Select For DRAM > 64MB	: Non-OS2		
		ESC : Quit	↑↓←→ : Select Item
		F1 : Help	PU/PD/+- : Modify
		F5 : Old Values (Shift)	F2 : Color
		F6 : Load BIOS Defaults	
		F7 : Load Setup Defaults	

CPU Internal Cache

This category enables CPU internal cache to speed up memory access.

External Cache

This category enables external cache to speed up memory access.

Quick Power On Self Test

This category speeds up Power On Self Test (POST) after you power on the computer. If it is set to Enabled, BIOS will shorten or skip some check items during POST.

Boot Sequence

This category determines which drive computer searches first for the disk operating system. Default value is A, C.

Swap Floppy Drive

When this category enables, the BIOS will swap floppy drive assignments so that Drive A: will function as Drive B: and Drive B: as Drive A:.

Boot Up Floppy Seek

During POST, BIOS will determine if the floppy disk drive installed is 40 or 80 tracks.

Boot Up NumLock Status

When this option enabled, BIOS turns on **Num Lock** when system is powered on so the end user can use the arrow keys on both the numeric keypad and the keyboard.

Boot Up System Speed

This option sets the speed of the CPU at system boot time. The settings are **High** or **Low**.

Gate A20 Option

When this category sets to Normal, the A20 signal is controlled by keyboard controller. When this category sets to Fast, the A20 signal is controlled by post 92 or chipset specific method.

Security Option

This category allows you to limit access to the system and Setup, or just to Setup.

When **System** is selected, the system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.

When **Setup** is selected, the system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

PS/2 Mouse Control Function

This category to set the PS/2 mouse be used or not. If there a PS/2 mouse attached to your system, this category must be enabled, if not, please disabled this category to release IRQ12.

PCI VGA Palette Snoop

This category must be set to enabled if there is any ISA VGA adapter card installed in the system, and disabled if there is any PCI VGA adapter card installed in the system.

OS Select For DRAM > 64MB

If there over 64MB memory on your system, please set this category to **OS2** for total memory detection under OS/2 operating system, otherwise set to **Non-OS2**.

Video BIOS Shadow/XXXXX-XXXXX Shadow

These categories determine whether Video BIOS and optional ROM will be copied to RAM.

Chipset Features Setup

ROM PCI/ISA BIOS (2A59CH2C)
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC.

DRAM RAS# Precharge Time : 4	PCI Concurrency : Enabled
DRAM R/W Leadoff Timing : 8/6	PCI Streaming : Enabled
DRAM RAS To Cas Delay : 3	PCI Bursting : Enabled
DRAM Read Burst Timing : x3333	Onboard FDD Controller : Enabled
DRAM Write Burst Timing : x3333	Onboard Serial Port 1 : COM1/3F8
System BIOS Cacheable : Disabled	Onboard Serial Port 2 : COM2/2F8
Video BIOS Cacheable : Disabled	Infra Red (IR) Function : Disabled
8 Bit I/O Recovery Time : 3	IR Transfer Mode : Half-Dup
16 Bit I/O Recovery Time : 2	Onboard Parallel Port : 378H/IRQ7
IDE HDD Block Mode : Enabled	Onboard Parallel Mode : ECP+EPP
IDE Primary Master PIO : Auto	ECP Mode Use DMA : 3
IDE Primary Slave PIO : Auto	
IDE Secondary Master PIO : Auto	
IDE Secondary Slave PIO : Auto	
On-Chip Primary PCI IDE: Enabled	ESC : Quit f1++ : Select Item
On-Chip Secondary PCI IDE: Enabled	F1 : Help PU/PD/+/- : Modify
PCI Slot IDE 2nd Channel : Enabled	F5 : Old Values <Shift>F2 : Color
	F6 : Load BIOS Defaults
	F7 : Load Setup Defaults

DRAM RAS# Precharge Time

This category set the DRAM RAS Precharge Timing. The options are **4** and **3**CLKs.

DRAM R/W Leadoff Timing

This category set the RAS DRAM Read/Write Leadoff timings for page/row miss cycles. The options are **8/6** and **7/5**CLKs.

DRAM RAS To CAS Delay

This category set the DRAM RAS to CAS Delay to controls the DRAM page miss and row miss leadoff timings. The options are **3** and **2**CLKs.

DRAM Read Burst Timing

This category set the DRAM Read Burst Timing. The timing used depends on the type of DRAM (standard page mode or EDO burst mode) on a per-bank basis. The options are **x4444**, **x3333**, and **x2222**.

DRAM Write Burst Timing

This category set the DRAM Write Burst Timing. The timing used depends on the type of DRAM (standard page mode or EDO burst mode) on a per-bank basis. The options are **x4444**, **x3333**, and **x2222**.

System BIOS Cacheable

This category allows the user to set whether the system BIOS F000~FFFF areas are cacheable or non-cacheable.

Video BIOS Cacheable

This category allows the user to set whether the video BIOS C000~C7FF areas are cacheable or non-cacheable.

8 Bit I/O Recovery Time

This category is used to add additional recovery delay between CPU or PCI master originated 8-bit I/O cycles to the ISA Bus. The options are **1, 2, 3, 4, 5, 6, 7, 8,** and **NA**.

16-Bit I/O Recovery Time

This category is used to add additional recovery delay between CPU or PCI master originated 16-bit I/O cycles to the ISA Bus. The options are **1, 2, 3, 4, 5, 6, 7, 8,** and **NA**.

IDE HDD Block Mode

This category is used to set IDE HDD Block Mode. If your IDE Hard Disk supports block mode, then you can enable this function to speed up the HDD access time. If not, please disable this function to avoid HDD access error.

IDE Primary Master PIO

In this category, there are five modes defined in manual mode and one automatic mode. There are **0, 1, 2, 3, 4,** and **AUTO**. The default settings for on board Primary Master PIO timing is Auto.

IDE Primary Slave PIO

In this category, there are five modes defined in manual mode and one automatic mode. There are **0, 1, 2, 3, 4,** and **AUTO**. The default settings for on board Primary Slave PIO timing is Auto.

IDE Secondary Master PIO

In this category, there are five modes defined in manual mode and one automatic mode. There are **0, 1, 2, 3, 4,** and **AUTO**. The default settings for on board Secondary Master PIO timing is Auto.

IDE Secondary Slave PIO

In this category, there are five modes defined in manual mode and one automatic mode. There are **0, 1, 2, 3, 4**, and **AUTO**. The default settings for on board Secondary Slave PIO timing is Auto.

On-Chip Primary PCI IDE

This category is used to defined on chip Primary PCI IDE controller is "**Enable**" or "**Disable**" setting.

On-Chip Secondary PCI IDE

This category is used to defined on chip Secondary PCI IDE controller is "**Enable**" or "**Disable**" setting.

PCI Slot IDE 2nd Channel

This category is used to defined add-on PCI IDE secondary controller is "**Enable**" or "**Disable**" setting.

PCI Concurrency

This category is used to defined PCI Concurrency is "**Enable**" or "**Disable**" setting.

PCI Streaming

This category is used to defined PCI Streaming is "**Enable**" or "**Disable**" setting.

PCI Bursting

This category is used to defined PCI Bursting is "**Enable**" or "**Disable**" setting.

Onboard FDC Control

This category specifies onboard floppy disk drive controller. This setting allows you to connect your floppy disk drives to the onboard floppy connector. Choose the "Disabled" settings if you have a separate control card.

Onboard Serial Port 1

This category is used to define onboard serial port 1 to **COM1/3F8H, COM2/2F8H, COM3/3E8H, COM4/2E8H** or **Disabled**.

Onboard Serial Port 2

This category is used to define onboard serial port 2 to **COM1/3F8H, COM2/2F8H, COM3/3E8H, COM4/2E8H, Disabled**.

Infra Red (IR) Function

HOT-541 main board support IrDA(HPSIR) and Amplitudes Shift Keyed IR(ASKIR) infrared through COM 2 port. This category specifies onboard Infra Red mode to **HPSIR, ASKIR** or **Disabled**.

IR Transfer Mode

This category specifies onboard infrared transfer mode to **full-duplicate** or **half-duplicate**.

Onboard Parallel Port

This category specifies onboard parallel port address to **378H, 278H, 3BCH** or **Disabled**.

Onboard Printer Mode

This category specifies onboard parallel port mode. The options are **EPP**(Extended Parallel Port), **ECP**(Extended Capabilities Port), Extended, and Compatible.(Extended Capabilities Port), Extended, and Compatible.

ECP Mode Use DMA

This category specifies DMA (Direct Memory Access) channel when ECP device is in use. The options are DMA **1** and DMA **3**.

Power Management Setup

BOM PCI/ISA BIOS (2A59CH2E)
POWER MANAGEMENT SETUP
AWARD SOFTWARE, INC.

Power Management	: Disable	IRQ3 (COM 2)	: ON
PM Control by APM	: Yes	IRQ4 (COM 1)	: ON
Video Off Method	: V/H SYNC+Blank	IRQ5 (LPT 2)	: OFF
Doze Mode	: Disable	IRQ6 (Floppy Disk)	: OFF
Standby Mode	: Disable	IRQ7 (LPT 1)	: OFF
Suspend Mode	: Disable	IRQ8 (RTC Alarm)	: OFF
HDD Power Down	: Disable	IRQ9 (IRQ2 Redir)	: OFF
IRQ3 (Wake-Up Event):	ON	IRQ10 (Reserved)	: OFF
IRQ4 (Wake-Up Event):	ON	IRQ11 (Reserved)	: OFF
IRQ8 (Wake-Up Event):	OFF	IRQ12 (PS/2 Mouse)	: ON
IRQ12 (Wake-Up Event):	ON	IRQ13 (Coprocesor)	: OFF
IRQ14 (Hard Disk)	: ON	IRQ15 (Reserved)	: OFF
Power Down Activities		ESC : Quit	↑↓+ : Select Item
COM Ports Accessed	: ON	F1 : Help	PU/PD/+/- : Modify
LPT Ports Accessed	: ON	F5 : Old Values (Shift)	F2 : Color
Drive Ports Accessed	: OFF	F6 : Load BIOS Defaults	
		F7 : Load Setup Defaults	

Power Management

This category determines the options of the power management function. Default value is Disable. The following pages tell you the options of each item & describe the meanings of each options.

- Disabled** Global Power Management will be disabled.
- User Define** Users can configure their own power management.
- Min Saving** Predefined timer values are used such that all timers are in their maximum value.
- Max Saving** Predefined timer values are used such that all timers minimum value.

PM Control by APM

If this category set to No, system BIOS will ignore APM when power is managing the system.

If this category setup to Yes, system BIOS will wait for APM's prompt before it enter any PM mode e.g. **DOZE**, **STANDBY** or **SUSPEND**.

Video Off Method

- Blank Screen** The system BIOS will only blanks off the screen when disabling video.
- V/H SYN +Blank** In addition to Blank Screen, BIOS will also turn off the V-SYNC & H-SYNC signals from VGA cards to monitor.

PCI Configuration Setup

ROM PCI/ISA BIOS (2A59CH2E)
PCI CONFIGURATION SETUP
AWARD SOFTWARE, INC.

PnP BIOS Auto-Config: Disabled	
Slot 1 Using INT# : AUTO	
Slot 2 Using INT# : AUTO	
Slot 3 Using INT# : AUTO	
Slot 4 Using INT# : AUTO	
1st Available IRQ : 9	
2nd Available IRQ : 11	
3rd Available IRQ : 10	
4th Available IRQ : 12	
PCI IRQ Activated By : Level	
PCI IDE IRQ Map To : PCI-AUTO	
Primary IDE INT# : A	
Secondary IDE INT# : B	
ESC : Quit	↑↓←→ : Select Item
F1 : Help	PU/PD/+/− : Modify
F5 : Old Values	(Shift)F2 : Color
F6 : Load BIOS Defaults	
F7 : Load Setup Defaults	

PnP BIOS Auto-Config

If enable this category, system BIOS will auto config Add-on devices under operating system that support PnP function.

Slot x Using INT#

The options in these categories are AUTO, A, B, C and D.

AUTO : BIOS will ask the PCI device which INT# does it want to use for interrupt ,check out which IRQ is available from the above and tell the device which IRQ has been assigned to it.

A, B, C, D : These options are reserved for "Dirty" cards from which the system BIOS cannot tell which INT it use!

Note :

1. Choose "AUTO" for all devices unless you know exactly which card is a dirty device & which INTs does that card uses!
2. Choose only "AUTO" for multifunction PCI devices because options A, B, C, D will force the BIOS to assign IRQs for function 0 only!

1st Available IRQ

The system BIOS will assign these available IRQs to the first found PCI device. The available options are **5, 7, 9, 10, 11, 12, 14, 15** and **NA**.

2nd Available IRQ

The system BIOS will assign these available IRQs to the second found PCI device. The available options are **5, 7, 9, 10, 11, 12, 14, 15** and **NA**.

3rd Available IRQ

The system BIOS will assign these available IRQs to the third found PCI device. The available options are **5, 7, 9, 10, 11, 12, 14, 15** and **NA**.

4th Available IRQ

The system BIOS will assign these available IRQs to the fourth found PCI device. The available options are **5, 7, 9, 10, 11, 12, 14, 15** and **NA**.

PCI IRQ Activated by

To tell the chipset the IRQ signals input is level or edge trigger.

PCI IDE IRQ Map to

The options in this category are : PCI-AUTO, PCI-SLOTx, ISA.

PCI-AUTO : The system BIOS will scan for PCI IDE devices & determine the location of the PCI IDE device.

PCI-SLOTx (x=1~4) : The BIOS will assign IRQ 14 for primary IDE INT#, and IRQ 15 for secondary IDE INT# for the specified slot.

ISA : The BIOS will not assign any IRQs even if PCI IDE card is found. Because some IDE cards connect the IRQ 14 & 15 directly from ISA slot through a extended cord. (this cord is called Legacy Header)

Primary IDE INT#

To tell which INT# does the primary IDE port on PCI IDE card is using for its interrupts.

Secondary IDE INT#

To tell which INT# does the secondary IDE port on PCI IDE card is using for its interrupts.

Password Setting

When you select this function, the following message will appear at the center of the screen to assist you in creating a password.

ENTER PASSWORD

ROM PCI/ISA BIOS (2A59CH2A)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC.

STANDARD CMOS SETUP	IDE HDD AUTO DETECTION
BIOS FEATURES SETUP	PASSWORD SETTING
CHIPSET FEATURES SETUP	SAVE & EXIT SETUP
POWER MANAGEMENT SETUP	EXIT WITHOUT SAVING
PCI CONFIGURATION SETUP	
LOAD BIOS DEFAULTS	Enter Password: *****
LOAD SETUP DEFAULTS	
Esc : Quit	↑ ↓ → ← : Select Item
F10 : Save & Exit Setup	(Shift)F2 : Change Color
Change/Set/Disable Password	

Type the password, up to eight characters, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password.

To disable password, just press <Enter> when you are prompted to enter password. A message will confirm the password being disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

PASSWORD DISABLED

If you select System at Security Option of BIOS Features Setup Menu, you will be prompted for the password every time the system is rebooted or any time you try to enter Setup. If you select Setup at Security Option of BIOS Features Setup Menu, you will be prompted only when you try to enter Setup.

Warning : Retain a safe record of your password. If you've forgotten or loosed the password, the only way to access the system is to clear CMOS memory, please refer to "Clear CMOS" or "Clear Password " section on chapter 2.