tion, key information provided upon key operation of a keyboard (not shown), and other miscellaneous information via various interfaces I/F (not shown). The multi type I/O port 14 receives performance information in the form of the MIDI information or the key information KBD. In the present embodiment, it is assumed that the performance information may be generated by an automatic performance program. In this case, the automatic performance program means that the performance information is generated in time series by a certain automatic sequence program. Therefore, the arrangement shown in Figure 1 works not only as a musical sound generator but also a sequencer. The type of I/F may be a serial or parallel port, RS-232C, RS-422 and so on. Especially in case of RS-232C, the computer system communicates with a host station through a public telephone network by a modem (not shown). Thus, the input source of the performance information may be the keyboard in case that the keyboard operation information is provided, or an external device connected through the I/F in case that the MIDI information is provided, or a sequence program executed by the CPU in case that the automatic performance information is provided. Numeral 15 denotes a storage unit, which is comprised of FD (Floppy Disk) or HD (Hard Disk). The storage unit 15 further stores application programs and data. Numeral 16 denotes a display which is composed of CRT or LCD (Liquid Crystal Display). The display 16 presents various data under the control of the CPU 10. Numeral 17 denotes an optional co-processor which executes floating point computation instead of the CPU 10. The rest of data processing is carried out by the CPU 10. Numeral 18 denotes a timer which counts time in timer processing described later. Numeral 19 denotes a DMAC (Direct Memory Access Controller) which transfers data to and from RAM 20 directly without the control by CPU. Nowadays, the co-processor 17, timer 18 and DMAC 19 may be accommodated in a single chip together with CPU 10, though these are discrete devices in the present embodiment. Numeral 20 denotes a RAM which has a structure similar to the first-mentioned RAM 13 with respect to its hardware construction. However, the RAM 13 is used as a work area for the program execution by the CPU, while the other RAM 20 is a waveform memory which temporarily stores a waveform represented by wave data. Numeral 21 denotes a DSP (Digital Signal Processor) for use in digital signal processing required for musical sound synthesis. Numeral 22 denotes an optional sound source which constitutes a first waveform generator of one chip LSI for generating a waveform of the musical sound according to performance information. Numeral 23 denotes a D/A converter which is enabled when a flag DACENBL is set to "1". Before the D/A converter 23, an FIFO data buffer (not shown) is normally provided. The wave data stored in the FIFO is read out at a sampling frequency fs. After the D/A converter 23, an LPF (Low Pass Filter) is normally provided (not shown). A cutoff frequency of the LPF is set to about half of the sampling frequency fs. The LPF is an output device of the musical sound generator. The musical sound is reproduced through an amplifier and a speaker. Numeral 24 denotes a RAM which is structured similarly to the RAM 13 or 20 with respect to its hardware construction. The RAM 24 is utilized as a work memory for the arithmetic operation of the DSP 21. Numeral 25 denotes a waveform memory which stores wave data of basic or typical timbres in case that the sound source 22 generates a musical sound according to a waveform memory readout method. The role of the waveform memory 25 and the RAM 20 is slightly different in a manner that the waveform memory 25 is used mainly by the sound source 22 and is provided in the form of ROM or a daughter board, while the RAM 20 is utilized by the CPU 10 as a waveform memory.

**[0010]** Generally in the arrangement above, some devices such as co-processor 17, DSP 21, sound source 22, RAM 24, and waveform memory 25 are often optionally installed according to user's choice. If the RAM 24 is not installed, a certain area of the RAM 13 is allocated for the DSP 21. The waveform memory 25 may not be installed if the sound source 22 is an FM synthesizing device which generates a musical sound by pure computation of wave data. The CPU 10 recognizes whether these optional devices are installed or not. In the present embodiment, the CPU 10 recognizes the existence of the optional devices according to one of methods listed below:

(1) A port address is reserved for a corresponding device connection. The CPU 10 accesses the port address immediately after power-on or reset of the system. If the CPU 10 detects a predetermined sign from the port address, it recognizes the existence of the corresponding device.

(2) A jumper switch is provided for signifying the device installation. The user turns the switch on at the time of installing the corresponding device.

(3) If the system is implemented as a personal computer, the optional devices are registered in a configuration file in terms of corresponding device drivers or in a batch file. The system software recognizes the devices through these files.

**[0011]** All these optional devices are fully installed and connected to the data bus 12 in the present embodiment. However, the connection port is not limited to the data bus 12. The optional devices may be connected via serial/parallel interfaces, through which each device carries out data transaction mutually with the CPU 10. In other words, any kind of interface is possibly provided for the optional devices, provided that the device can communicate with the CPU through the interface. For example, the sound source 22 may actually be provided