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(54) Hardware or software architecture implementing self-biased conditioning

(57) An architecture, which may be embodied in hardware, software or a combination of the two, implementing self-biased conditioning and having at least one primary response network (1) comprising: a single activation node (X) responding to a first value of an input signal received from at least one sensor (S_A) by outputting a trigger signal (O_1), one or more motor centres (M) receiving the trigger signal (O_1) and having an innate response to generate an output signal (O_3) for activating an actuator (C_1), means (y^+, y^-) for applying positive and negative reinforcement signals to the motor centre (M) to promote or inhibit the response of the motor centre (M) to the trigger signal (O_1), one or more expectation nodes (Y) receiving an input signal from at least one second sensor (S_B), and generating an output signal (O_2) indicating when the generation of said output signal (O_3) for activating the actuator is not appropriate; and an associative memory (2) generating said positive and negative reinforcement signals in response to a determination that the response of the motor centre requires promotion or inhibition.

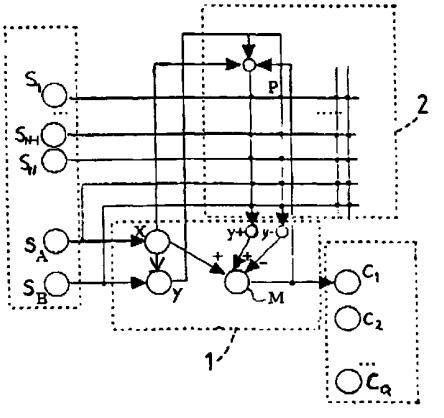

FIG.1

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