Protel 99

SmartTeam TECHNOLOGY

SmartDoc TECHNOLOGY

SmartTool TECHNOLOGY

Designed for Microsoft® Windows NT® Windows 98

Protel®
Making Electronic Design Easy™

Versatile schematic or CUPL-based

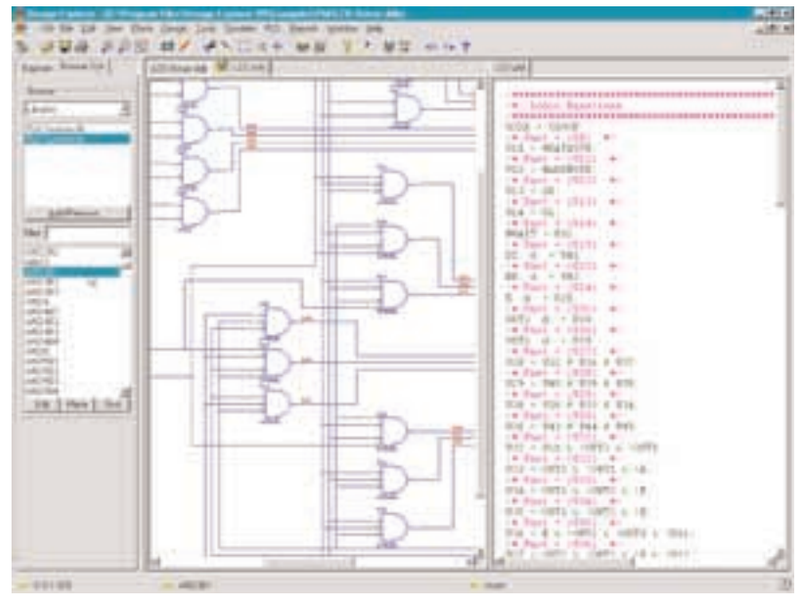
Protel 99's integrated PLD editor is a versatile and powerful development environment that can be used to create sophisticated logic designs for Programmable Logic Devices (PLDs). Enter the design as a schematic, or code it in the industry-standard CUPL hardware description language. Protel 99 will produce all the files necessary to program and test the device. A perfect solution for all PLD and CPLD design jobs.

Universal device support

New programmable logic devices seem to appear every day and you need design tools that keep pace. Protel 99's PLD Compiler is device and manufacturer independent, allowing you to target a wide range of PLDs. With Protel you're not locked into a particular device vendor, so you can choose the perfect device for your design needs. And you won't need to learn a new development environment each time you target a different device type.

Not sure how big your design will be? Simply elect to compile for a "virtual" device and you can create and test your design before choosing the final target PLD.

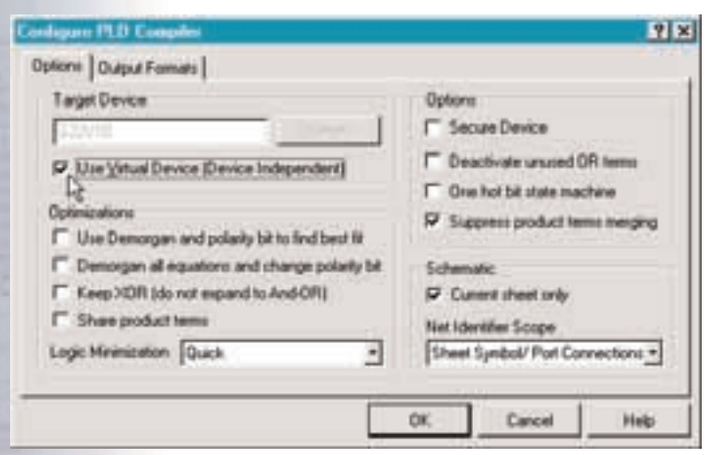
Protel 99's PLD compiler gives you total programmable logic design freedom.



Protel 99 comes supplied with a comprehensive PLD schematic symbol library that makes it easy to capture and compile your PLD design as a schematic. Alternatively, you can describe your circuit using the industry-standard CUPL hardware description language in Protel 99's built-in text editor, which includes full CUPL syntax highlighting support.

Choose your design methodology

Because Protel 99 gives you a choice of PLD design entry methods you can choose the design methodology that suits your needs. Create your PLD as a schematic or enter the description directly using the CUPL hardware description language – the choice is yours.



Protel 99's PLD Compiler supports compilation for a "virtual" device, allowing you to create and test your design before choosing the final target PLD.

Schematic-based PLD design

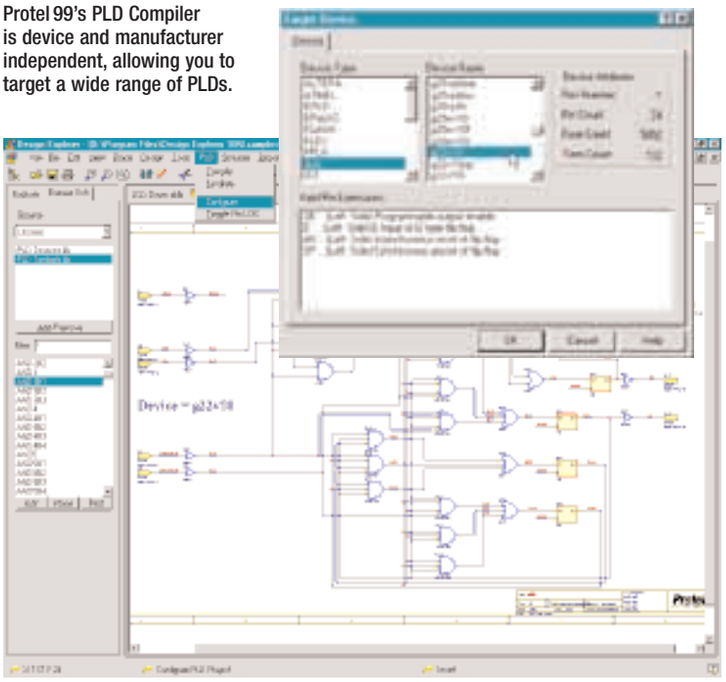
Protel 99 comes with a comprehensive logic library that allows you to compile your PLD design directly from a schematic. Simply create your schematic using components from the PLD Symbols library, select your target device, and press the Compile button. The schematic is translated into a CUPL PLD file, then compiled to produce the download file. Schematic-based PLD design, with full support for multi-sheet hierarchical projects, brings the benefits of graphical design entry to the world of PLDs.

CUPL HDL

CUPL is a simple-to-learn yet powerful hardware description language that has become an industry standard for PLD design. Use Protel 99's syntax-aware text editor to easily create CUPL-based PLD designs directly. CUPL supports high-level language constructs, such as: expression substitution for equations; shorthand notation for lists, address ranges, and bit fields; Boolean equations; truth tables; and state machines. The text editor integrates directly with Protel 99's PLD compiler and provides full debugging support.

programmable logic design

Protel 99's PLD Compiler is device and manufacturer independent, allowing you to target a wide range of PLDs.



Fast and powerful compiler

Protel 99's PLD Compiler uses the fastest and most powerful minimizer available for programmable logic equation reduction, with four levels of minimization. The Compiler simplifies Boolean expressions using the distributive property and DeMorgan's Theorem, allowing you to implement your design in the most cost-effective way. Compilation or simulation errors are automatically highlighted in the source file, with a full description of the error condition available in a comprehensive compiler report.

The Compiler produces industry-standard JEDEC program files, ready to download directly to a device programmer. Get your design into silicon faster with Protel 99.

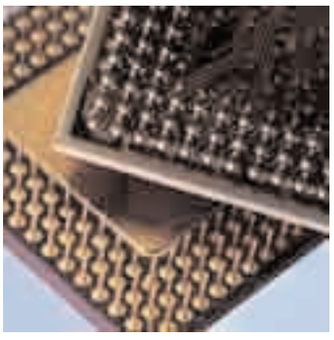
Protel 99 includes an integrated functional PLD simulator. Simply define your test vectors and Protel 99 will show you the device waveforms using its integrated waveform viewer. Protel 99's simulation syntax supports high-level language concepts, such as conditional looping, conditional simulation, arithmetic and random vector generation, and multiple order statements. As well, verified test vectors can be downloaded to your logic programmer for physical testing of the device after programming.

Immediate simulation and design verification

Be sure your design will work first time with Protel 99's integrated functional PLD simulator. Simply define your test vectors and Protel 99 will show you the device waveforms using its integrated waveform viewer, which displays the results in an easy-to-understand spreadsheet-style window.

Change the order of the waveforms, use color to highlight a signal and create a bus from a set of signals – the simulation viewer gives you the full performance picture.

Protel 99's simulation syntax supports high-level language concepts, such as conditional looping, conditional simulation, arithmetic and random vector generation, and multiple order statements. As well, verified test vectors can be downloaded to your logic programmer for physical testing of the device after programming. Integrate programmable logic into your design the easy way with Protel 99's PLD creation and simulation tools.



Feature Highlights

- *Universal device support, including a large library of generic devices*
- *Device-independent CUPL Hardware Description Language*
- *Advanced Compiler incorporating fast and powerful logic minimization algorithms, including Quine-McClusky*
- *Compile and generate download files directly from Protel 99's Schematic Editor*
- *Simulation waveform viewer, supporting signal buses, timing marks and direct measurement*
- *Produces an industry-standard JEDEC download file, as well as other manufacturer-specific formats*
- *Syntax-aware Text Editor with integrated error reporting*
- *Includes specialized fitters for; Altera Max, AMD MACH, Atmel High Density EPLDs, Cypress, Intel FLEX, ICT EPLD/FPGA's, Lattice, National MAPL, Motorola, Philips PML, Xilinx EPLD*

Specifications

Download formats:
JEDEC, POF, PRG, HL (Signetics IFL devices), ASCII hex

Output formats:

Palasm PDS, Expanded Macro MX, Berkely PLA, Xilinx XNF, PDIF, EDIF

Minimization methods:
Quick, Quine McClusky, Presto, Expresso

Contact your local sales office today for your FREE Protel 99 30-Day Trial CD.