W H I T E P A P E R

AMD Athlon™ Processor System Bus

The First 200MHz System Bus for x86 Computing Platforms: Delivering Unprecedented System Bandwidth and Scalable Performance

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Introduction: Enabling the Highest System Bandwidth for x86 Platforms

The computing industry is rapidly advancing the state-of-the-art in high-performance system platforms and peripherals. These advances are driving the need to significantly enhance the data movement bandwidth of the x86 system architecture. Improvements to legacy system buses have now doubled PCI bus speeds from 33 to 66 MHz and increased AGP bus speeds from 66 to 133 MHz. Advanced technologies, such as Rambus and DDR memory and IEEE 1394 are being incorporated into system designs. System OEMs and hardware developers are also leading the way in creating new, high-bandwidth bus technologies, such as PCI-X and Future I/O, which are capable of providing more than 1 Gbyte/sec peak data movement bandwidth.

Although sixth-generation processors have increased core operating frequencies to 1000 MHz and have added dedicated instructions to accelerate data movement, the crucial system bus remains between 66 MHz and 133 MHz. This provides a peak data movement bandwidth of 1.06 Gbytes/sec at 133 MHz with a sustained data movement bandwidth being much lower due the sixth-generation bus protocol. This relatively small bus bandwidth is inadequate to meet the needs of the emerging high-bandwidth technologies, as illustrated in Figure 1 below.

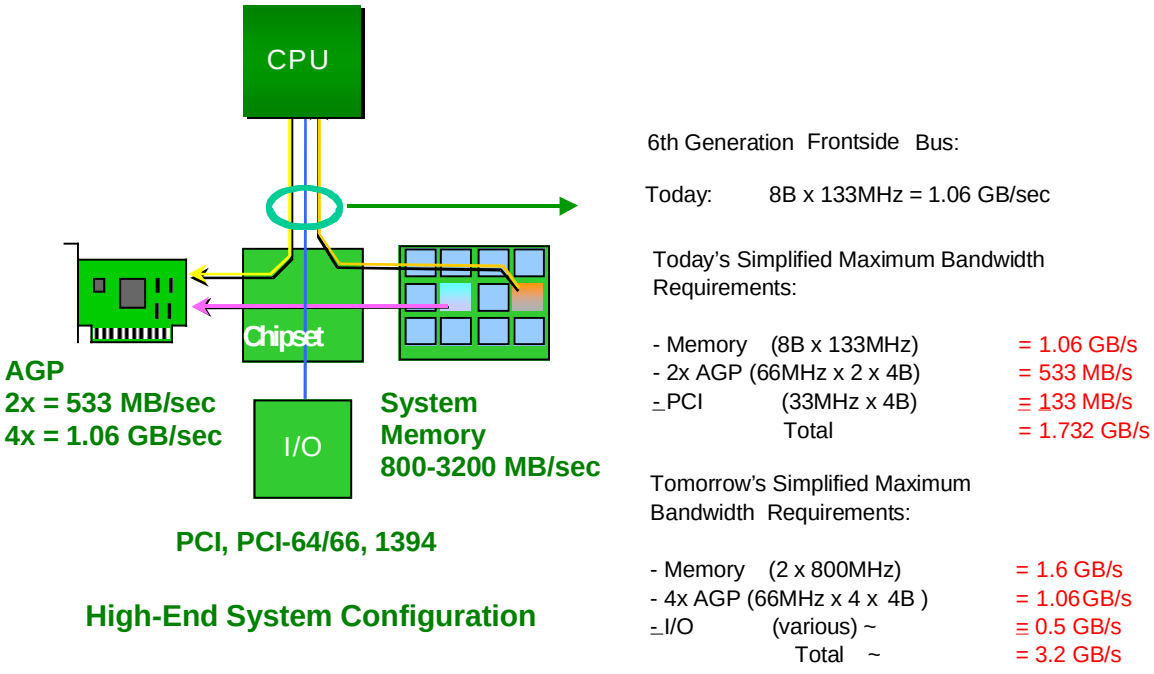


Figure 1: Today's and Tomorrow's Maximum Bandwidth Requirements

To meet today's and tomorrow's system bandwidth requirements, the x86 processor architecture and system bus must be revolutionized. To meet this challenge, AMD has designed the seventh-generation AMD Athlon™ processor to include the most advanced system bus architecture ever implemented in an x86 processor, delivering the highest system bandwidth for x86 computing platforms.

AMD's high-performance, scalable, and cost-effective bus implementation for the AMD Athlon processor is based on the Alpha™ EV6 bus technology licensed from Digital Equipment Corporation. AMD selected this advanced technology to enable optimal implementations of the AMD Athlon processor in x86 platforms ranging from high-end desktop systems to uniprocessor and multiprocessor workstations and servers.

The AMD Athlon processor system bus, operating at 200 MHz, is capable of delivering 1.6 Gbytes/sec data bandwidth, and it can scale to 3.2 Gbytes/sec data bandwidth at 400 MHz. As the first 200MHz bus for x86 platforms, the AMD Athlon processor system bus provides scalable bandwidth and next-generation features that are not available from other platforms based on 133MHz bus implementations or even enhanced older generation x86 processors such as Intel's Pentium® III processor.

AMD Athlon™ Processor System Bus Architecture Overview

The AMD Athlon processor system bus architecture is designed to deliver unprecedented data movement bandwidth for next-generation x86 platforms, as well as the high performance and reliability required by enterprise-class application software running on multiprocessing servers. The system bus architecture consists of three high-speed channels (a unidirectional processor request channel, a unidirectional snoop channel, and a 72-bit bidirectional data channel, including 8-bit error code correction [ECC] protection), source synchronous clocking, and a packet-based protocol. The interface signals use a HSTL-like, low-voltage swing signaling technology contained within the Slot A mechanical connector.

The initial AMD Athlon processor product implementation includes a 200MHz system bus that delivers up to 50 percent more peak bandwidth than any other x86 system bus. As the AMD Athlon processor's clock frequency increases, the system bus frequency can also increase to provide even greater data bandwidth for larger, more powerful system configurations. Because the AMD Athlon processor system bus uses source synchronous clocking, it can achieve data rates of more than 400 MHz, resulting in 3.2 Gbytes/sec peak data bandwidth.

The AMD Athlon processor system bus uses a packet-based protocol instead of the limited pipelined P6 bus protocol to transfer processor requests to the system chipset. A packet-based protocol minimizes system bandwidth utilization and supports a greater

number of outstanding transactions so that the processor rarely waits for critical system data. The AMD Athlon processor system bus allows each processor to have 24 outstanding transactions—three times as many transactions as the newer Intel Pentium III processors.

Applications that depend on critical data from system memory will directly benefit from the larger 64-byte burst transfers and ECC protection of all data enabled by the high-speed AMD Athlon processor system bus. In addition, the AMD Athlon processor system bus architecture is capable of accessing more than 8 terabytes of physical addressable memory compared to 64 gigabytes supported by the Intel P6 bus architecture. These and other system bus advantages are listed in Table 1 below. By combining the next-generation architecture of the AMD Athlon processor with AMD's new high-speed system bus architecture, high-performance x86 platforms based on the AMD Athlon processor can deliver superior performance, features, and scalability for data-intensive and transaction-based applications.

Table 1. 200-MHz AMD Athlon™ Processor System Bus Advantages

	AMD Seventh Generation	Intel Previous Generation	AMD Previous Generation
Feature	AMD Athlon™	Pentium® III	AMD-K6®-III
Number of pins	242	242	321
Bus operating frequency	200 to 400+ MHz	66 to 133 MHz	66 to 100 MHz
Data bus width	64 bits	64 bits	64 bits
Data bus integrity	8-bit ECC	8-bit ECC	Parity
Clock Technology	Source synchronous	Common	Common
Peak bandwidth	1.6 to 3.2 GB/s+	533 MB/s to 1.06 GB/s	533 MB/s to 800 MB/s
Multiprocessing	Yes, point-to-point	Yes, shared	Yes, shared
Max. system processors	Unlimited (by chipset)	Unlimited (by chipset)	Unlimited (by chipset)
Dedicated snoop channel	Yes	No	No
Cache Control Policy	MOESI/MESI	MESI	MESI
Outstanding transactions	24 per processor	4-8 per processor	2 total
Machine check architecture	Yes	Yes	Yes
Physical memory support	8 TB*	64 GB	4 GB
Burst transaction size	64 byte	32 byte	32 byte

*The size of supported physical memory depends on the specific processor and chipset implementation.

Higher Bandwidth with Source Synchronous Clocking

Dramatic improvements in data movement bandwidth are enabled by an innovative clocking technique used in the AMD Athlon processor called "source synchronous clocking." This clocking technique allows data to be transferred on a point-to-point, high-speed channel between the processor and system logic.

With source synchronous clocking transfers, the sender (such as the processor) provides a high-speed clock along with the data to the receiver so that the clock and data are received at the same time, independent of the motherboard transport delay and signal routing. Because the clock and data both travel the same length and routing through the motherboard, the frequency of source synchronous transfers is not limited by the amount of time it takes the data to travel from the sender to the receiver, like that of the "common-clock" method used by the Intel P6 bus.

With common-clock transfers, there is only one clock between the sender and receiver that all transfers must use. This common clock typically operates at a slow frequency, such as 133 MHz, due to the transport delay on the motherboard—the amount of time it takes the data to travel from the sender to the receiver. However, the AMD Athlon processor system bus is supported by multiple independent, high-speed clocks dedicated for request and data transfers, thereby delivering fast transfers to and from the processor.

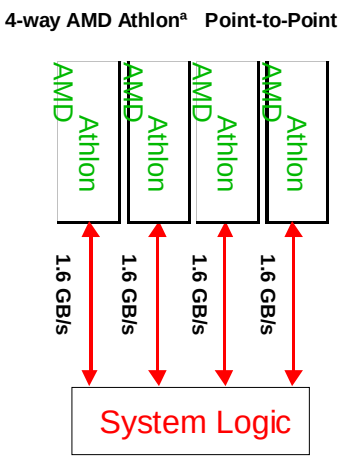
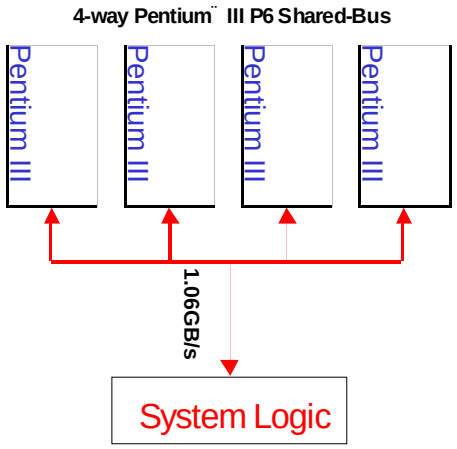
Server-Class Processor System Bus Features

The AMD Athlon processor system bus architecture offers features and capabilities specifically designed for high-performance workstation and server configurations. Among its numerous "server-class" features, the AMD Athlon processor system bus architecture uses high-speed, point-to-point, source synchronous channels instead of the older, slower common-clock, shared-bus technology used in the Intel P6 bus architecture. (See Table 2 on the following page for comparison of bus features.)

Source synchronous channels offer many advantages over common-clock, shared-bus technology, such as fewer signal pins for low-cost packages or packages with multiple channels, as well as point-to-point connections that are electrically cleaner than buses, thus permitting higher bus frequencies. Thus, applications running on workstations and servers can immediately benefit from the significant increase in data bandwidth enabled by the AMD Athlon processor system bus architecture.

Because the AMD Athlon processor system bus architecture uses a point-to-point topology for all channels, the system bus does not suffer the potential performance drawbacks of a shared-bus topology used in the Intel P6 bus architecture. For example, if there are four Intel processors sharing a 133MHz Intel P6 bus capable of delivering 1GB/s of data bandwidth, each processor is limited to just 200MB/s of data bandwidth. With AMD's point-to-point bus topology, each AMD Athlon processor in a four-way system configuration has 1.6GB/s of data bandwidth—6.4 times the bandwidth of a four-way Intel P6 133MHz shared-bus topology.

Table 2: Processor Bus 4-Way Multiprocessing Bandwidth Comparison

AMD Seventh Generation AMD Athlon processor™ System Bus	Intel Previous Generation Pentium® III (P6) Bus
200-MHz bus bandwidth (up to 50% more peak bandwidth than any other x86 system bus), scalable to 400 MHz	133-MHz bus bandwidth
Point-to-point dedicated architecture based on Digital's Alpha™ EV6 technology – a superior, higher-bandwidth bus solution for multiprocessing platforms	Available bus bandwidth is shared, which limits clock frequency
Source synchronous clocking (clock forwarding)	Common clock limits frequency
1.6 Gbytes/sec per processor bandwidth for 4-way system configuration	250 Mbytes/sec per processor bandwidth for 4-way system configuration
24 outstanding transactions per processor	4-8 outstanding transactions per processor
	

The AMD Athlon processor system bus architecture uses 64-byte burst data transfers, thereby delivering up to 50 percent more peak bandwidth than any other x86 system bus. In addition to providing significantly higher data bandwidth, the AMD Athlon processor system bus enables more efficient cache utilization by defining a flexible cache control policy, which is managed by the system chipset. By including the cache control policy within the system chipset, chipset developers can design a variety of system-level features or configurations for different markets. The AMD Athlon processor system bus also implements a MOESI (Modify, Owner, Exclusive, Shared, Invalid) cache control policy—the first such implementation for x86 processors.

Since the AMD Athlon processor system bus has separate, dedicated high-speed channels for processor requests to the system and snoop requests from the system, AMD Athlon processors are not limited to the strict and long "arbitration-address transfer-snoop response-data transfer" protocol used by the Intel P6 bus. AMD Athlon processors can send up to 24 outstanding transfer packets—three times as many as the newer Intel P6

bus—to the system without waiting for a system response. This superior packet-transfer capability enhances the ability of AMD Athlon processor-based workstations and servers to provide uninterrupted service while running applications or performing data transfers.

In multiprocessing server configurations, snoop traffic can severely limit overall performance when using a strict protocol like the Intel P6 bus. The AMD Athlon processor is designed to not incur such performance limitations because each processor includes a dedicated channel for servicing snoops from the system.

For large enterprise server configurations, the AMD Athlon processor system bus architecture is designed to allow CPUs to access up to 8 terabytes of physical addressable memory, while Intel's P6 bus technology supports only 64 gigabytes of a physical memory. Since the AMD Athlon processor system bus uses packets over a high-speed request channel, more physical address bits can be implemented, allowing scalable, flexible design implementations.

AMD Athlon processors include a machine check architecture to allow system administrators to monitor system behavior and detect system-level failures before they impact end users. This machine check architecture provides a mechanism for software to detect and report hardware errors, such as external system bus errors and internal processor errors. The AMD Athlon processor system bus also provides full 8-bit ECC (Error Correction Code) protection for reliable data transfers to and from the system. ECC provides single-bit correction and multi-bit detection using the machine-check architecture.

Leveraging Existing Physical/Mechanical Infrastructure

Although the new AMD Athlon processor system bus requires a new motherboard implementation incorporating AMD's Slot A infrastructure, AMD has created a motherboard design that maintains considerable mechanical compatibility to the existing PC infrastructure. Slot A motherboards optimized for the AMD Athlon processors use the same mechanical design and connector as Intel's Slot 1, as well as standard PC-100 DRAM DIMMs, support for standard I/O buses (such as ISA, PCI, AGP, and USB), support for the standard keyboard, mouse, serial and parallel I/O, and support for readily available PC power supplies, fans, and hardware enclosures.

Summary: Higher Bandwidth and Scalable Headroom for the Future

When AMD began designing the world's first seventh-generation x86 processor, it became apparent that none of the current system buses offered the bandwidth needed for a new processor architecture that offered the ultimate performance for cutting-edge software applications. Furthermore, today's mainstream 133MHz system bus does not offer the

"headroom" to keep pace with the requirements of emerging high-bandwidth I/O and system memory technologies.

AMD's solution was to implement a new, high-speed system bus endowed with bandwidth-enhancing features, such as clock forwarding, MOESI cache coherency policy, and ECC protection—features that would complement the high clock speeds and industry-leading processing capabilities of the AMD Athlon processor.

Rather than creating an entirely new system bus design, AMD licensed Digital's high-performance Alpha™ EV6 interface technology for the AMD Athlon processor and implemented the x86 industry's first system bus operating at 200 MHz and delivering 1.6 Gbytes/sec data bandwidth (scalable to 3.2 Gbytes/sec at 400 MHz). By leveraging Alpha™ EV6 technology, the AMD Athlon processor offers superior performance and scalable headroom for today's and tomorrow's data-intensive, transaction-based applications. The AMD Athlon processor thus has a system bus architecture designed to support a full range of next-generation system platforms, from high-performance desktop systems to workstations to multiprocessing enterprise servers.

AMD Overview

AMD (NYSE: AMD) is a global supplier of integrated circuits for the personal and networked computer and communications markets. AMD produces processors, flash memories, and products for communications and networking applications. The world's second-leading supplier of Windows® compatible processors, AMD has shipped more than 120 million x86 microprocessors, including more than 90 million Windows compatible CPUs. Founded in 1969 and based in Sunnyvale, California, AMD has sales and marketing offices worldwide and manufacturing facilities in Sunnyvale; Austin, Texas; Dresden, Germany; Bangkok, Thailand; Penang, Malaysia; Singapore; and Aizu-Wakamatsu, Japan. AMD had revenues of $2.8 billion in 1999.

Cautionary Statement

This release contains forward-looking statements, which are made pursuant to the safe harbor provisions of the Private Securities Litigation Reform Act of 1995. Forward-looking statements are generally preceded by words such as "expects," "plans," "believes," "anticipates," or "intends." Investors are cautioned that all forward-looking statements in this document involve risks and uncertainty that could cause actual results to differ materially from current expectations. Forward-looking statements in this document about the AMD Athlon processor involve the risk that the AMD Athlon system bus will not support the requirements of next-generation system platforms; that AMD may not be successful in developing an infrastructure to support the processor; that third parties may not provide peripherals or the infrastructure to support the processor and the processor's system bus; and that the processor will not achieve customer and market acceptance. We urge investors to review in detail the risks and uncertainties in the company's Securities and Exchange Commission filings, including the most recently filed Form-10K.