

Index

A

- ABS
 - Store Absolute Value 12-23
- absolute branch 5-22
- ADD
 - Add Registers 12-24
- add with saturation 7-16
- ADDC
 - Add Register with Carry 12-25
- ADDI
 - Add Immediate
 - 16 bits 12-26
 - 32 bits 12-27
- ADDK
 - Add Constant (5 Bits) 12-28
- addressing 3-2-3-3
- ADDXY
 - Add Registers in XY Mode 12-29
- A-file registers 5-2
- airbrush effect 7-24
- ALU 1-7
- AND
 - AND Registers 12-30
- ANDI
 - AND Immediate (32 Bits) 12-31
- ANDN
 - AND Register with Complement 12-32
- ANDNI
 - AND Not Immediate (32 Bits) 12-33
- antialiasing 7-23
- applications 1-4
- array pitch 4-15

B

- background color register 5-17
- bank selection 11-25
- barrel shifter 1-7
- B-file registers 5-3, 5-5-5-19
- BLANK 2-9, 9-2
- blanking 2-9, 6-26, 6-28, 6-48, 6-50
- block diagram 1-6
- Boolean operations 7-17
- Boolean pixel processing 6-11
- Bresenham line algorithm 7-2, 7-10
- BTST
 - Test Register Bit
 - constant 12-34
 - register 12-35
- bulk initialization of VRAMs 9-19, 9-27
- bus request priorities 11-4
- bus request signal 2-10
- byte addressing 10-21
- byte alignment 12-9
- byte moves 12-9
- bytes 4-1
- B0 (SADDR) 5-7
- B1 (SPTCH) 5-8
- B10 (COUNT) 5-19
- B11 (INC1) 5-19
- B12 (INC2) 5-19
- B13 (PATTRN) 5-19
- B13 (TEMP) 5-19
- B2 (DADDR) 5-9
- B3 (DPTCH) 5-11
- B4 (OFFSET) 5-12
- B5 (WSTART) 5-13
- B6 (WEND) 5-14
- B7 (DYDX) 5-15
- B8 (COLOR0) 5-17
- B9 (COLOR1) 5-18

C

- C bit 5-21
- cache disable 6-12
- cache hit 5-25
- cache miss 5-25
- cache replacement algorithm 5-24
- CALL
 - Call Subroutine Indirect 12-36
- CALLA
 - Call Subroutine Absolute 12-37
- CALLR
 - Call Subroutine Relative 12-38
- Cartesian coordinates 4-15
- CAS 2-7, 11-2
- CD bit 5-26, 6-9, 6-12
- CF bit 5-26, 6-31, 6-32
- chip select pin 2-5
- clock timing logic 1-7
- CLR
 - Clear Register 12-39
- CLRC
 - Clear Carry 12-40
- CMP
 - Compare Registers 12-41
- CMPI
 - Compare Immediate
 - 16 bits 12-42
 - 32 bits 12-43
- CMPXY
 - Compare X and Y Halves of Registers 12-44
- Cohen-Sutherland algorithm 7-30
- color planes 7-12
- color-expand operation 7-5
- COLOR0 register 5-17
- COLOR1 register 5-18
- column address strobe 2-7
- compare point to window 7-3
- constant-to-register moves 12-8
- CONTROL 6-9
- CONTROL register 6-9
- CONVDP 7-4
- CONVDP register 4-12, 6-13
- conversion factor 6-13, 6-14
- CONVSP 7-4
- CONVSP register 4-12, 6-14
- COUNT register 5-19
- CPW
 - Compare Point to Window 12-45
- CVXYL
 - Convert XY Address to Linear Address 12-47

D

- DADDR register 5-9
- data enable pin 2-7
- data paths 1-7, 5-28
- data select pins 2-5
- data structures
 - bytes 4-1
 - fields 4-1, 4-2-4-5
 - pixel arrays 4-1
 - pixels 4-1, 4-6-4-10
- DDOUT 2-7, 11-2
- DEC
 - Decrement Register 12-49
- DEN 2-7, 11-2
- destination address register 5-9
- destination conversion factor 6-13
- destination pitch register 5-11
- development tools list 1-3
- DIE bit 6-39
- DINT
 - Disable Interrupts 12-50
- DIP bit 6-40
- display interrupt 8-4, 9-14
- display memory 9-19
- display pitch 4-10, 5-8, 5-11, 6-13, 6-14, 9-19
- DIVS
 - Divide Registers Signed 12-51
- DIVU
 - Divide Registers Unsigned 12-53
- dot rate 9-15
- DPTCH register 5-11, 6-13
- DPYADR register 6-15
- DPYCTL register 6-17
- DPYINT register 6-22
- DPYSTRT register 6-23
- DPYTAP register 6-24
- DRAM 6-9, 11-5
 - refresh cycles 6-9
 - refresh interval 6-45
 - refresh rate 6-9
- DRAM refresh 11-11, 11-12, 11-25
- DRAW
 - Draw and Advance 12-55
- draw and advance 7-10
- DSJ
 - Decrement Register and Skip Jump 12-58
- DUDATE bits 6-17, 6-18
- DXV bit 6-17, 6-20
- DYDX register 5-15

E

- EINT
 - Enable Interrupts 12-64
- EMU
 - Initiate Emulation 12-65
- emulation 2-10
- ENV bit 6-17
- EXAMPLE
 - Example Instruction 12-21
- EXGF
 - Exchange Field Size 12-66
- EXGPC
 - Exchange Program Counter with Register 12-67
- external interlaced video 9-18
- external interrupts 8-3
- external synchronization 9-16
- external video 6-17

F

- FE bit 4-2
- FE0 bit 5-20
- FE1 bit 5-20
- field moves 12-10
- field size 5-20, 5-21
- fields 4-1, 4-2-4-5
 - addressing 4-2
 - alignment 4-3
 - extraction 4-2
 - insertion 4-2, 4-5
 - size 4-2
- fill 7-5
 - Fill Array with Processed Pixels
 - linear 12-68
 - XY 12-72
- foreground color register 5-18
- FS0 4-2
- FS0 bits 5-20
- FS1 4-2
- FS1 bits 5-20
- function select pins 2-5

G

- general-purpose register files 1-6, 5-2-5-19
- GETPC
 - Get Program Counter into Register 12-77
- GETST
 - Get Status Register into Register 12-78
- graphics standards 1-2

H

- halt program execution 6-34
- HCOUNT register 6-25
- HCS 2-5, 10-2
- HD0-HD15 2-6, 10-2
- HEBLNK register 6-26
- HESYNC register 6-27
- HFS0, HFS1 2-5, 10-2
- HL bit 6-39
- HLBIT 2-6, 10-2
- HIP bit 6-40
- HLDA/EMUA 2-10
- HLDS 2-5, 10-2
- HLT bit 5-26, 6-2, 6-31, 6-34
- HOLD 2-10
- hold and emulation signals 2-4, 2-10
 - HLDA/EMUA 2-10
 - HOLD 2-10
 - RUN/EMU 2-10
- hold interface 11-18
- hold request 11-4
- horizontal front porch 9-5
- horizontal sync 2-9
- horizontal timing 9-12
- horizontal timing registers
 - HCOUNT 6-25, 9-4
 - HEBLNK 6-26, 9-4
 - HESYNC 6-27, 9-4
 - HSBLNK 6-28, 9-4
 - HTOTAL 6-38, 9-4
- horizontal video timing 9-6, 9-7
- host interface 10-1, 10-24
 - bandwidth 10-22
 - data transfer 10-9
 - indirect accesses of local memory 10-11
 - reads and writes 10-4
 - ready signal to host 10-8

- registers 6-6
 - HSTADRH 10-3
 - HSTADRH register 6-29
 - HSTADRL 6-30, 10-3
 - HSTCTL 10-3
 - HSTCTLH 6-31, 10-3
 - HSTCTLL 6-35, 10-3
 - HSTDATA 6-37, 10-3
 - selection 10-3
 - signals 10-2
 - timing examples 10-5
 - host interface bus pins 2-4, 2-5
 - HCS 2-5
 - HD0-HD15 2-6
 - HFS0,HFS1 2-5
 - HINT 2-6
 - HLDS 2-5
 - HRDY 2-5
 - HREAD 2-5
 - H~~IDS~~ 2-5
 - HWRITE 2-5
 - host interrupt 8-4
 - host read/write strobes 2-5
 - host-present mode 8-9, 8-12
 - HRDY 2-5, 10-2, 10-8
 - HREAD 2-5, 10-2
 - HSBLNK register 6-28
 - HSD bit 6-17
 - HSTADRH register 6-29
 - HSTADRL register 6-30
 - HSTCTLH register 6-31
 - HSTCTLL register 6-35
 - HSTDATA register 6-37
 - HSYNC 2-9, 6-20, 6-25, 9-2
 - HTOTAL register 6-38
 - H~~UDS~~ 2-5, 10-2
 - HWRITE 2-5, 10-2
- I**
- I/O registers 1-7, 6-1-6-51
 - addressing 6-2
 - at reset 6-2
 - host interface registers 6-6
 - interrupt interface registers 6-7
 - latency of writes 6-3
 - local memory interface registers 6-7
 - memory map 6-2
 - summary 6-4
 - video timing and screen refresh registers 6-8
 - IE bit 5-20
 - illegal opcode interrupts 8-8
 - illegal operand 8-4
 - implied graphics operands 5-5
 - INC
 - Increment Register 12-79
 - INCLK 2-7, 11-2
 - INCR bit 6-31, 6-33, 10-11
 - incremental algorithms 7-10
 - INCW bit 6-31, 6-34, 10-11
 - INC1 register 5-19
 - INC2 register 5-19
 - indirect accesses of local memory 10-11
 - indirect branch 5-22
 - input clock 2-7
 - instruction cache 1-7, 5-23-5-27
 - cache disable 6-12
 - cache flush 6-32
 - cache hit 5-25
 - cache miss 5-25
 - cache replacement algorithm 5-24
 - disabling 5-26
 - downloading new code 5-26
 - flushing 5-26
 - LRU stack 5-24
 - operation 5-25
 - P flag 5-25
 - segment miss 5-25
 - segments 5-24
 - SSA register 5-24
 - subsegment miss 5-25
 - instruction words 5-23
 - INTENB register 6-39
 - interlaced display 9-25
 - interlaced video 9-11, 9-18
 - internal interrupts 8-4
 - interrupt interface
 - registers 6-7
 - INTENB 6-39, 8-3
 - INTPEND 6-40, 8-3
 - interruptible instructions 7-9
 - interrupts 2-6, 8-1-8-7
 - display interrupt 6-22, 8-4, 9-14
 - enable bit 5-20
 - external interrupts 8-3
 - host interrupt 8-4
 - host interrupt request signal 2-6
 - IE bit 5-20
 - illegal opcode interrupts 8-8
 - illegal operand 8-4
 - INTENB 6-39
 - internal interrupts 8-4
 - interrupt request pins 8-3
 - interrupt requests 6-36
 - INTIN bit 6-36
 - INTOUT bit 6-36
 - INTPEND 6-40

Index

- local interrupt request signals 2-8
- nonmaskable interrupt 6-31, 6-32, 8-4
- priorities 8-1, 8-2, 8-4
- processing 8-5
- registers 8-3
- RESET 2-11
- stack operations 3-9
- vector addresses 8-2
- window interrupt 8-4
- intersecting rectangles 7-3
- INTIN bit 6-35, 6-36
- INTOUT bit 6-35, 6-36
- INTPEND register 6-10, 6-40

J

- JAcc
 - Jump Absolute Conditional 12-80
- JRcc
 - Jump Relative Conditional
 - long 12-84
 - short 12-82
- JUMP
 - Jump Indirect 12-86

K

- key features of the GSP 1-3

L

- LAD0-LAD15 2-8, 11-2
- LAL 2-7, 11-2
- LBL bit 6-31, 6-33
- LCLK1, LCLK2 2-8, 11-2
- LCSTRT bits 6-23
- LINE
 - Line Draw with XY Addressing 12-87
- line clipping 7-29
- linear addressing 4-10
- LINT1, LINT2 2-8, 8-3, 11-2
- LMO
 - Leftmost One 12-94
- LNCNT bits 6-15, 6-23
- local address/data bus 2-8
- local memory interface 11-1, 11-29

- addressing mechanisms 11-23
- hold interface timing 11-18
- I/O register access cycles 11-14
- internal cycles 11-13
- memory bus request priorities 11-4
- read cycle 11-8
- read-modify-write operations 11-15
- registers 6-7
 - CONTROL 6-9, 11-3
 - CONVDP 6-13, 11-3
 - CONVSP 6-14, 11-3
 - PMASK 6-42, 11-3
 - PSIZE 6-44, 11-3
 - REFCNT 6-45, 11-3
- shift-register-transfer cycles 11-9
- signals 11-2
- timing 11-5-11-22
- wait states 11-16
- write cycle 11-7

- local memory interface pins 2-4, 2-7

- CAS 2-7
- DDOUT 2-7
- DEN 2-7
- INCLK 2-7
- LAD0-LAD15 2-8
- LAL 2-7
- LCLK1, CLK2 2-8
- LINT1, LINT2 2-8
- LRDY 2-8
- RAS 2-7
- TR/QE 2-7
- W 2-7

- local read/write strobes 2-7

- logical pixels 4-6

- LRDY 2-8, 11-2

M

- MAX operation 7-16
- memory bus request priorities 11-4
- memory map 3-4
- message buffers 6-35, 6-36
- microcontrol ROM 1-7
- midpoint subdivision 7-30
- MIN operation 7-16
- MMFM 12-9
 - Move Multiple Registers from Memory 12-95
- MMTM 12-9
 - Move Multiple Registers to Memory 12-97
- MODS
 - Modulus Signed 12-99

Index

MODU

Modulus Unsigned 12-100

MOVB 12-9

Move Byte Instruction

absolute to absolute 12-110
absolute to register 12-109
indirect to indirect 12-105
indirect to register 12-104
indirect with displacement to indirect with displacement 12-107
indirect with displacement to register 12-106
register to absolute 12-103
register to indirect 12-101
register to indirect with displacement 12-102

MOVE 12-8, 12-10

Move Field

absolute to absolute 12-139
absolute to indirect (postincrement) 12-137
absolute to register 12-135
indirect (postincrement) to indirect (postincrement) 12-123
indirect (postincrement) to register 12-121
indirect (predecrement) to indirect (predecrement) 12-127
indirect (predecrement) to register 12-125
indirect to indirect 12-120
indirect to register 12-119
indirect with displacement to indirect (postincrement) 12-131
indirect with displacement to indirect with displacement 12-133
indirect with displacement to register 12-129
register to absolute 12-118
register to indirect 12-113
register to indirect (postincrement) 12-114
register to indirect (predecrement) 12-115
register to indirect with displacement 12-116

Move Register to Register 12-112

summary 12-8

MOVI 12-8

Move Immediate

16 bits 12-141

32 bits 12-142

MOVK 12-8

Move Constant (5 Bits) 12-143

MOVX 12-8

Move X Half of Register 12-144

MOVY 12-8

Move Y Half of Register 12-145

MPYS

Multiply Registers Signed 12-146

MPYU

Multiply Registers Unsigned 12-148

MSGIN bits 6-35

MSGOUT bits 6-35, 6-36

multiple register moves 12-9

multiple-GSP systems 9-16

N

N bit 5-21

NEG

Negate Register 12-150

NEGB

Negate Register with Borrow 12-151

NIL bit 6-17, 6-20

NMI bit 6-31

non-branch 5-22

noninterlaced video 9-9

nonmaskable interrupt 6-7, 6-31, 8-4

nonmaskable interrupt mode 6-32

NOP

No Operation 12-152

NOT

Complement Register 12-153

O

OFFSET register 4-12, 5-12

on-screen memory 9-19

OR

OR Registers 12-154

ORG bit 6-17, 6-19

ORI

OR Immediate (32 Bits) 12-155

outcode 7-30

output clocks 2-8

P

- P flag 5-25
 - panning 9-26
 - PATTRN register 5-19
 - PBH bit 6-9, 6-10
 - PBV bit 6-9, 6-11
 - PBX bit 5-21
 - PC 5-22
 - pick window 7-26
 - picture elements 4-6
 - pin descriptions 2-2
 - pinout 2-2
 - pitch 7-4
 - pitch conversion factors 4-12
 - PIXBLT
 - Pixel Block Transfer
 - Pixel Block Transfer Instruction
 - binary to linear 12-156
 - binary to XY 12-161
 - linear to linear 12-168
 - linear to XY 12-174
 - XY to linear 12-180
 - XY to XY 12-185
 - PixBlt direction 6-11
 - PixBlts 4-14, 7-4
 - pixel array 4-14
 - pixel block transfers 4-14, 7-4
 - pixel processing 6-11, 7-15
 - pixels 4-1, 4-6-4-10
 - addressing 4-6
 - on the screen 4-7
 - pixel size 6-44
 - PSIZE register 6-44
 - representation in a register 4-6
 - size 4-6
 - storage in memory 4-7
 - XY addressing 4-7
- PIXT
- Pixel Transfer Instruction
 - indirect to indirect 12-198
 - indirect to register 12-196
 - indirect XY to indirect XY 12-202
 - indirect XY to register 12-200
 - register to indirect 12-191
 - register to indirect XY 12-193
 - summary 12-14
 - plane mask 7-12
 - plane masking 6-42

- PMASK register 6-42
- POPST
 - Pop Status Register from Stack 12-205
- postclipping 7-29
- PP bit 6-9
- PPOP bits 6-11
- preclipping 7-29
- program counter 1-6, 5-22
- PSIZE register 4-12, 6-44
- PUSHST
 - Push Status Register onto Stack 12-206
- PUTST
 - Copy Register into Status 12-207

R

- RAS 2-7, 11-2
- REFCNT register 6-45
- references 1-10
- register file A 5-2
- register file B 5-3, 5-5-5-19
- register-to-register moves 12-8
- relative branch 5-22
- replace operation 7-18
- RESET 2-11, 8-9-8-12
 - effect on cache 5-24
 - effect on GSP registers 8-10
 - effect on instruction cache 8-10
 - effects on I/O registers 6-2
 - HLT bit 6-34
- RETI
 - Return from Interrupt 12-208
- RETS
 - Return from Subroutine 12-209
- REV
 - Store Revision Number 12-210
- RINTVL bits 6-45
- RL
 - Rotate Left
 - constant 12-211
 - register 12-212
- row address strobe 2-7
- row and column addressing 11-6
- ROWADR bits 6-45
- RR bit 6-9
- RUN/EMU 2-10

S

SADDR register 5-7
 scan line counter 6-15
 screen origin 4-8, 6-17, 6-19
 screen refresh 6-20, 6-23, 9-1-9-27
 screen refresh enable 6-17
 screen size limits 9-3
 screen-refresh address 6-15
 screen-refresh cycles 9-19
 segment miss 5-25
 self-bootstrap mode 8-9, 8-11
 self-modifying code 5-26
 SETC
 Set Carry 12-213
 SETF
 Set Field Parameters 12-214
 SEXT
 Sign Extend to Long 12-215
 shift register transfer enable pin 2-7
 shift register transfers 6-17
 sign (N) bit 5-21
 SLA
 Shift Left Arithmetic
 constant 12-216
 register 12-217
 SLL
 Shift Left Logical
 constant 12-218
 register 12-219
 software traps 8-8
 source address register 5-7
 source conversion factor 6-14
 source pitch register 5-8
 SP 3-6, 5-2, 5-4
 SPTCH register 5-8, 6-14
 SRA
 Shift Right Arithmetic
 constant 12-220
 register 12-221
 SRE bit 6-17, 6-20
 SRFADR bits 6-15, 6-23
 SRL
 Shift Right Logical
 constant 12-222
 register 12-223
 SRSTRT bits 6-23
 SRT bit 6-17, 6-19
 SSA register 5-24
 ST 5-20
 stack 3-6-3-11
 multiple-register operations 3-9
 operation during a subroutine 3-9
 operation during interrupts 3-9

 structure 3-7
 32-bit register operations 3-8
 stack pointer 5-2, 5-4
 starting address of array 4-14, 7-7
 starting corner selection 7-7
 status register 1-6, 5-20-5-21
 strobes 10-4
 SUB
 Subtract Registers 12-224
 SUBB
 Subtract Registers with Borrow 12-225
 SUBI
 Subtract Immediate
 16 bits 12-226
 32 bits 12-227
 SUBK
 Subtract Constant 12-228
 subsegment miss 5-25
 subtract with saturation 7-16
 SUBXY
 Subtract Registers in XY Mode 12-229

T

T bit 6-9
 tap point register 6-24
 TEMP register 5-19
 $\overline{TR}/\overline{OE}$ 2-7, 11-2
 transparency 7-11
 enabling (T bit) 6-10
 TRAP 8-8
 Software Interrupt 12-230
 traps 8-8
 two-dimensional arrays 4-14, 7-4

V

V bit 5-21
 and window checking 7-25
 VCLK 2-9, 9-2
 VCOUNT register 6-22, 6-47
 VEBLNK register 6-48
 vector addresses 8-2
 vertical front porch 9-5
 vertical sync 2-9
 vertical timing registers
 VCOUNT 6-47, 9-4
 VEBLNK 6-48, 9-4

Index

- VESYNC 6-49, 9-4
- VSBLNK 6-50, 9-4
- VTOTAL 6-51, 9-4
- vertical video timing 9-8-9-13
- VESYNC register 6-49
- video clock 2-9
- video enable 6-17
- video timing 9-1-9-27
- video timing and screen refresh
 - display address 6-15, 6-17
 - display interrupt 6-22
 - registers 6-8
 - DPYADR 6-15
 - DPYCTL 6-17
 - DPYINT 6-22
 - DPYSTRT 6-23
 - DPYTAP 6-24
 - HCOUNT 6-25, 9-4
 - HEBLNK 6-26, 9-4
 - HESYNC 6-27, 9-4
 - HSBLNK 6-28, 9-4
 - HTOTAL 6-38, 9-4
 - VCOUNT 6-47, 9-4
 - VEBLNK 6-48, 9-4
 - VESYNC 6-49, 9-4
 - VSBLNK 6-50, 9-4
 - VTOTAL 6-51, 9-4
 - video timing signals 9-2
- video timing signals 2-4, 2-9
 - BLANK 2-9
 - HSYNC 2-9
 - VCLK 2-9
 - VSYNC 2-9
- VRAM 11-5
- VRAMs 6-8, 9-19
 - bulk initialization 9-27
 - tap point address 6-24
- VBLNK register 6-50
- VSYNC 2-9, 6-20, 9-2
- VTOTAL register 6-51

W

- W 2-7, 11-2
- W bit 6-9, 6-10
- WEND register 5-14
- window checking 4-15, 6-10, 7-25
- window clipping 7-27
- window end address register 5-14

- window hit detection 7-26
- window interrupt 8-4
- window miss detection 7-27
- window start address register 5-13
- windows 5-13, 5-14
 - WEND register 5-14
 - WSTART register 5-13
- WSTART register 5-13
- WVE bit 6-39
- WVP bit 6-40

X

- XOR
 - Exclusive OR Registers 12-232
- XORI
 - Exclusive OR Immediate Value 12-233
- XY addressing 4-8, 4-10, 4-11, 4-13, 5-15
 - benefits 4-11
 - DYDX register 5-15
 - format 4-11
 - OFFSET register 5-12
 - XY-to-linear conversion 4-11, 6-13, 6-14
- XY register moves 12-8
- X1E bit 6-39
- X1P bit 6-40
- X2E bit 6-39
- X2P bit 6-40
- X3E bit 6-39
- X3P bit 6-40

Z

- Z bit 5-21
- ZEXT
 - Zero Extend to Long 12-234