

## B. Emulation Guidelines for Prototyping

The TMS34010 XDS<sup>1</sup> (Extended Development Support) emulator is a self-contained system that provides full-speed, in-circuit emulation of the TMS34010. The *TMS34010 XDS/22 Emulator User's Guide* provides detailed information about XDS operation and use. This appendix provides guidelines for using the TMS34010 in a prototyping environment.

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### B.1 Synchronizing a Host Processor with the TMS34010

The following guidelines will help you integrate a TMS34010 XDS emulator into a system that contains a host processor and a GSP. The prototype target system may or may not contain an emulator for the host processor:

- In a prototype system that contains *an actual host processor* instead of an emulator for the host processor, the host may have to avoid initiating accesses of the GSP's host interface registers while the GSP emulator is halted on a breakpoint condition.
- If emulators are present for *both the host processor and GSP*, the two emulators may need to be synchronized to each other to permit a breakpoint in one emulator to halt both emulators. Without this capability, debugging software that performs communication between the host and GSP may be difficult.

If the TMS34010 emulator halts on a breakpoint and the host attempts to access the GSP's host interface, the XDS will prevent the access by intercepting the chip-select signal to the emulator (so that HCS remains inactive high) and by transmitting a not-ready signal (HRDY low) to the host. This forces the host to wait (by extending the access cycle) until the TMS34010 emulator begins running again. Host processors that cannot tolerate lengthy waits caused by not-ready signals should not attempt to access the GSP's host interface registers while the emulator is halted. For instance, if the host bus must be available to perform DRAM-refresh cycles at regular intervals, a long access (extended by a not-ready signal from the GSP) could delay refreshing for so long that data in memory becomes corrupted.

While the TMS34010 emulator is halted, host accesses of GSP registers must be prevented in order for the GSP to maintain a valid internal state while halted. When the TMS34010 emulator encounters a breakpoint, it stops execution and dumps an image of its internal registers to a buffer memory in the XDS. This image can be inspected and altered. When the emulator enters run mode again, the internal register image is loaded back into the GSP internal registers, and execution continues. During the time the TMS34010 emulator is halted, the host is not allowed to modify the state of the internal registers because this would invalidate the register image.

Consider a prototype system that contains an actual host processor and a TMS34010 emulator. The host system can monitor the  $\overline{\text{HLDA}}/\overline{\text{EMUA}}$  signal from the XDS to determine when the TMS34010 emulator halts on a breakpoint. To allow this, the  $\overline{\text{HLDA}}/\overline{\text{EMUA}}$  signal should be connected to one of the host processor's interrupt request inputs. An active low  $\overline{\text{HLDA}}/\overline{\text{EMUA}}$  signal will interrupt the host. Once interrupted, the host must not attempt to access the GSP's host interface registers until  $\overline{\text{HLDA}}/\overline{\text{EMUA}}$  goes inactive high again. One method of ensuring this is for the host's interrupt routine to repeatedly poll the  $\overline{\text{HLDA}}/\overline{\text{EMUA}}$  signal until it goes high.

If a host access of a GSP register is in progress when a GSP breakpoint occurs, the XDS will allow the access to complete before driving  $\overline{\text{HLDA}}/\overline{\text{EMUA}}$  active low. The XDS will allow the access in progress to complete normally; the HRDY signal to the host from the TMS34010 emulator will not be forced low by the XDS.

In a prototype system that contains a host processor emulator and TMS34010 emulator, the two emulators may need to be synchronized to permit simultaneous breakpointing. This may be necessary, for example, when software running on the host signals to software on the GSP to begin a graphics operation. When the host emulator reaches a breakpoint immediately following the point at which it signals the GSP, the GSP should also breakpoint. Otherwise, you may have difficulty observing the operation performed by the GSP in response to the signal from the host.

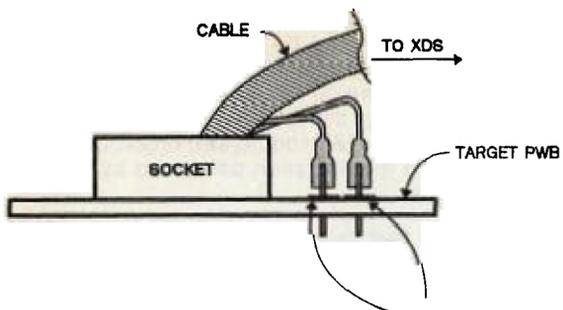
Similarly, a breakpoint condition that causes the TMS34010 emulator to halt should also halt the host emulator. Assume, for example, that a portion of GSP software is being debugged that signals the host-resident software to perform an operation. If the TMS34010 emulator halts on a breakpoint just following its signal to the host, the host emulator should also halt. Otherwise, you may have difficulty observing the operation performed by the host in response to the signal from the GSP.

Two pins on the XDS/22 target system connector facilitate synchronization of the host and TMS34010 emulators:

- The  $\overline{\text{RUN/EMU}}$  input is pulled low to halt the TMS34010 emulator.  $\overline{\text{RUN/EMU}}$  can be controlled by the host emulator so that when it halts on a breakpoint, the TMS34010 emulator is also halted.
- The  $\overline{\text{HLDA/EMUA}}$  output goes low when the GSP emulator halts on a breakpoint condition. This signal can be connected to the host emulator, causing it to halt as well.

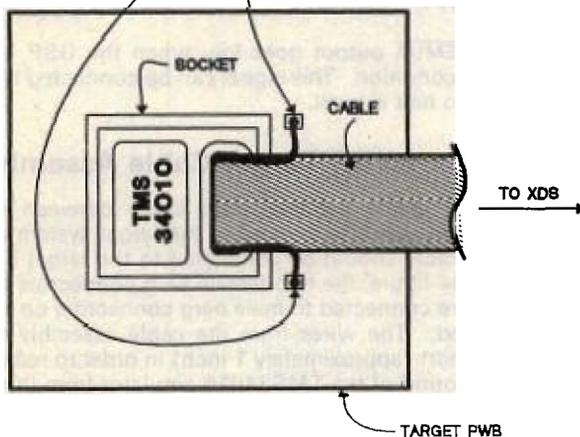
### B.2 Proper Grounding of XDS Target Cable Assembly

To ensure that a low impedance path exists between the ground of the TMS34010 emulator and the ground of the target system prototype, the XDS target cable assembly should be connected to the target ground as shown in Figure B-1. In the figure, the two female berg connectors emanating from the cable assembly are connected to male berg connectors on the target PWB that are well grounded. The wires from the cable assembly to the female berg connectors are short (approximately 1 inch) in order to reduce the inductances separating the ground of the TMS34010 emulator from the target ground.



PLACE FEMALE CONNECTOR FROM XDS TARGET CABLE ASSEMBLY OVER MALE CONNECTOR STAFF ON PWB, WHICH ARE CONNECTED TO THE GROUND OF THE ASSET SYSTEM

a. Side View



b. Top View

Figure B-1. Grounding the XDS Target Cable Assembly